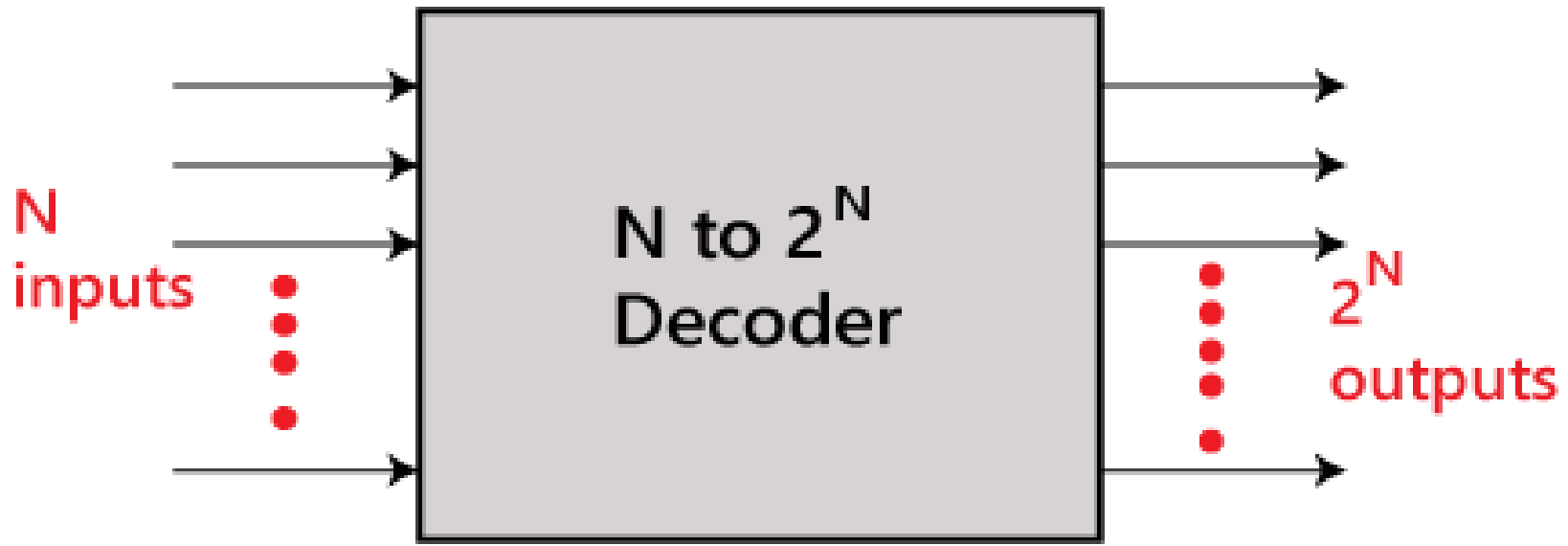
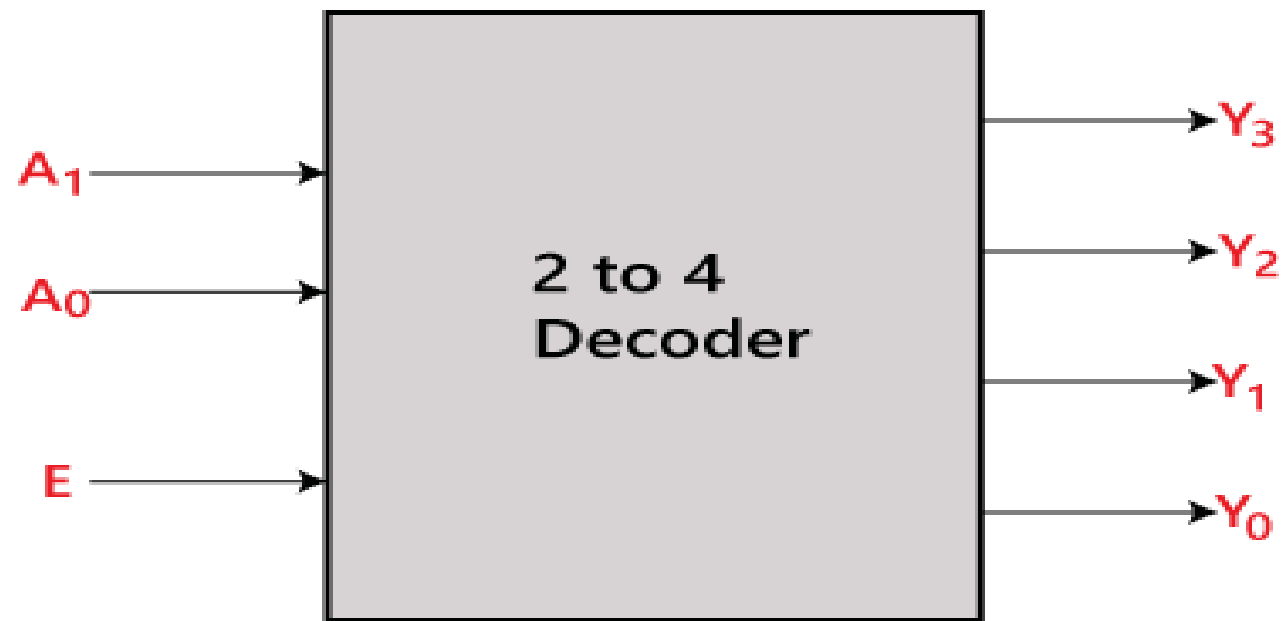


Decoder

The combinational circuit that change the binary information into 2^N output lines is known as **Decoders**. The binary information is passed in the form of N input lines. The output lines define the 2^N -bit code for the binary information. At a time, only one input line is activated for simplicity. The produced 2^N -bit output code is equivalent to the binary information.

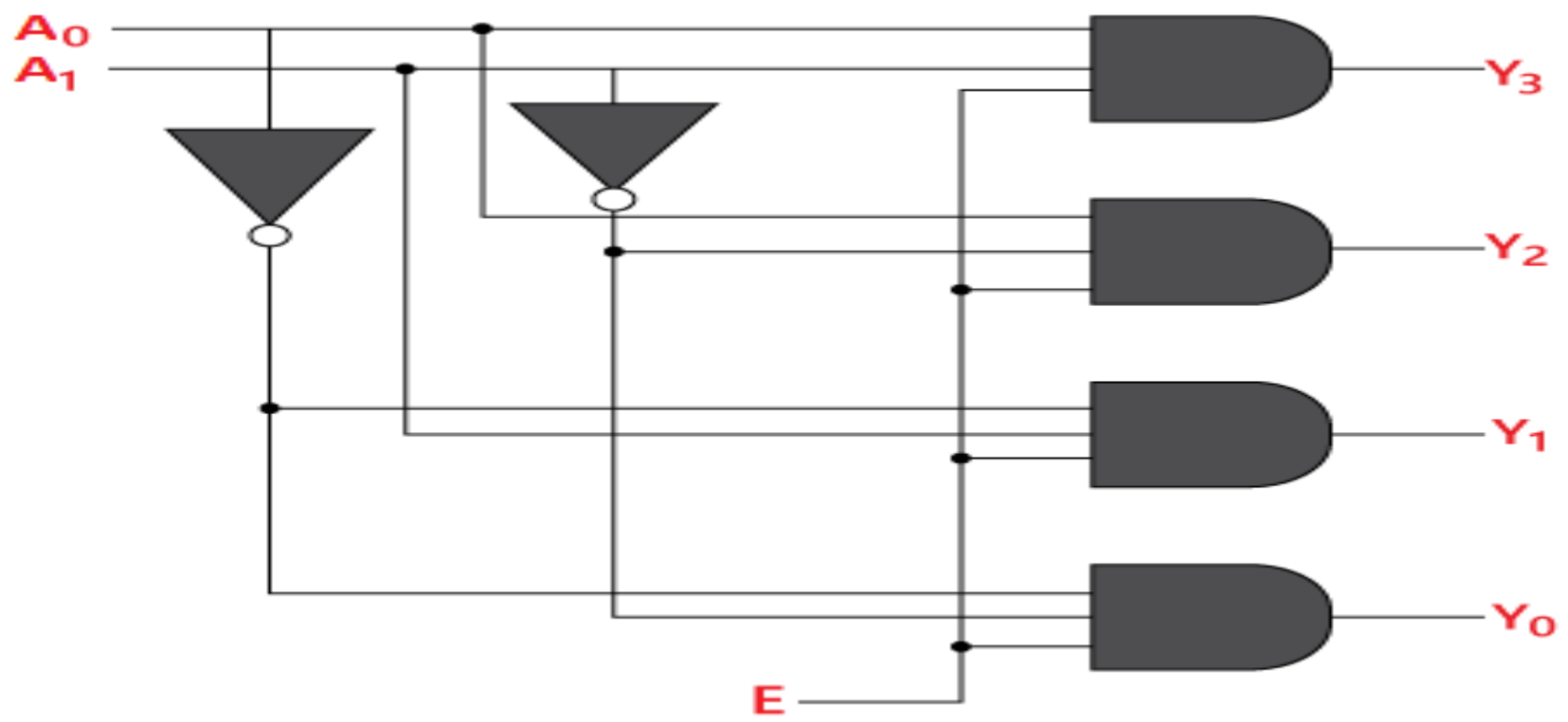


- 2 to 4 line decoder:
- In the 2 to 4 line decoder, there is a total of three inputs, i.e., A_0 , and A_1 and E and four outputs, i.e., Y_0 , Y_1 , Y_2 , and Y_3 . For each combination of inputs, when the enable 'E' is set to 1, one of these four outputs will be 1.



Enable	INPUTS		OUTPUTS			
E	A₁	A₀	Y₃	Y₂	Y₁	Y₀
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

- The logical expression of the term Y_0 , Y_1 , Y_2 , and Y_3 is as follows:
- $Y_3 = E \cdot A_1 \cdot A_0$
 $Y_2 = E \cdot A_1 \cdot A_0'$
 $Y_1 = E \cdot A_1' \cdot A_0$
 $Y_0 = E \cdot A_1' \cdot A_0'$
- Logical circuit of the above expressions is given below:



3 to 8 line decoder:

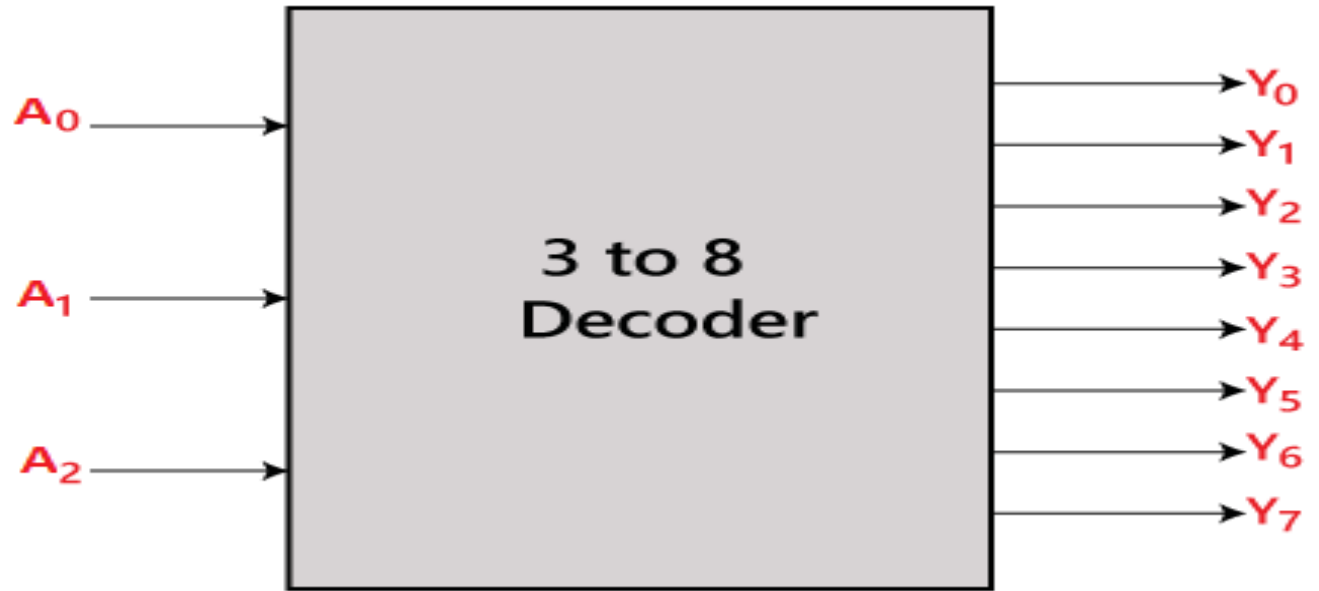
The 3 to 8 line decoder is also known as **Binary to Octal Decoder**.

In a 3 to 8 line decoder, there is a total of eight outputs, i.e., Y_0 , Y_1 , Y_2 , Y_3 , Y_4 , Y_5 , Y_6 , and Y_7

and three outputs, i.e., A_0 , A_1 , and A_2 . This circuit has an enable input 'E'.

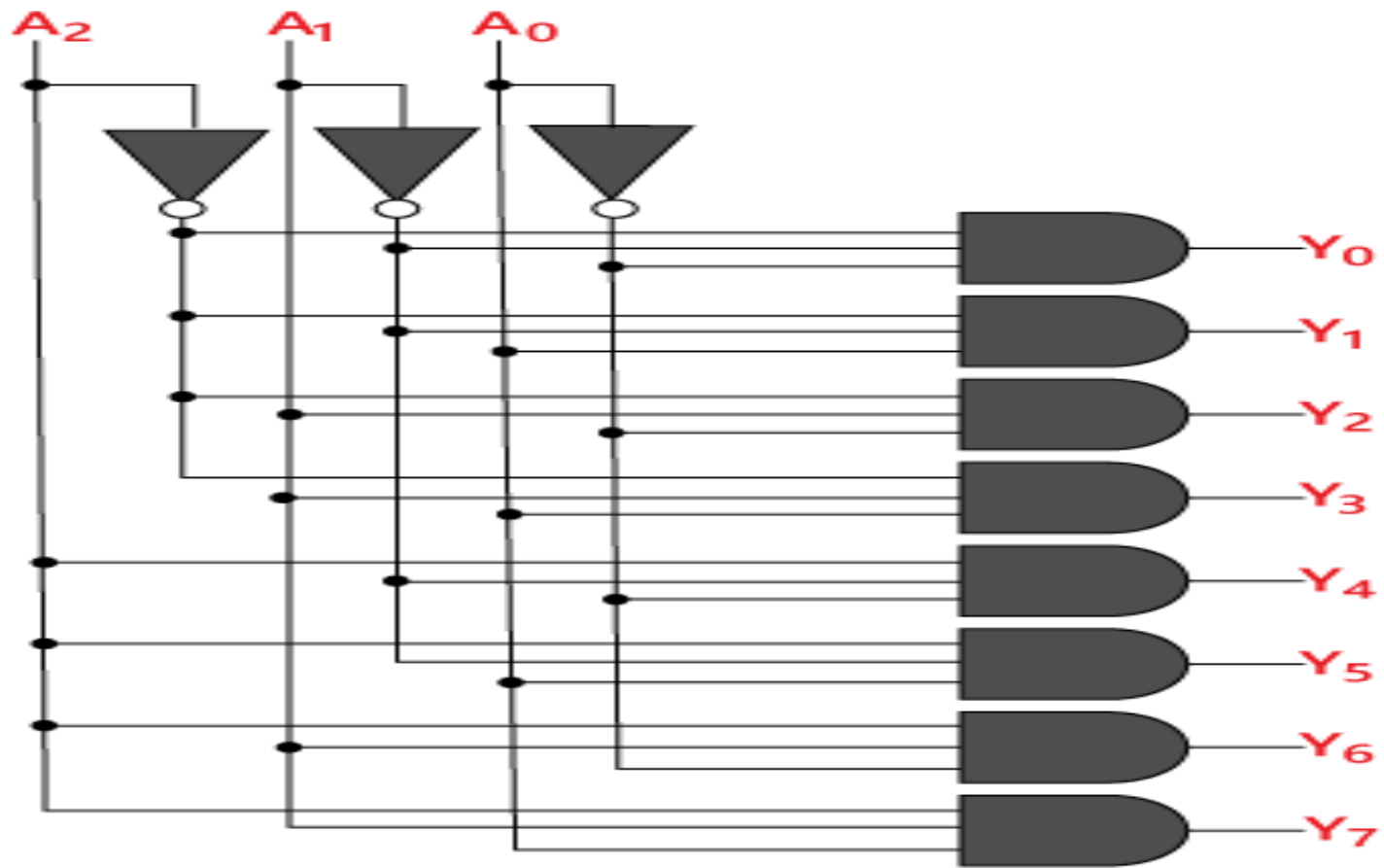
Just like 2 to 4

line decoder, when enable 'E' is set to 1, one of these four outputs will be 1.



Enable	INPUTS			Outputs							
E	A₂	A₁	A₀	Y₇	Y₆	Y₅	Y₄	Y₃	Y₂	Y₁	Y₀
0	x	x	x	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

- The logical expression of the term $Y_0, Y_1, Y_2, Y_3, Y_4, Y_5, Y_6,$ and Y_7 is as follows:
- $Y_0 = A_0' \cdot A_1' \cdot A_2'$
- $Y_1 = A_0 \cdot A_1' \cdot A_2'$
- $Y_2 = A_0' \cdot A_1 \cdot A_2'$
- $Y_3 = A_0 \cdot A_1 \cdot A_2'$
- $Y_4 = A_0' \cdot A_1' \cdot A_2$
- $Y_5 = A_0 \cdot A_1' \cdot A_2$
- $Y_6 = A_0' \cdot A_1 \cdot A_2$
- $Y_7 = A_0 \cdot A_1 \cdot A_2$



4 to 16 line Decoder

In the 4 to 16 line decoder,

there is a total of 16 outputs,

i.e., $Y_0, Y_1, Y_2, \dots, Y_{16}$ and four inputs, i.e., $A_0, A_1, A_2,$ and A_3 .

The 3 to 16 line decoder can be constructed using either 2 to 4 decoder or 3 to 8 decoder.

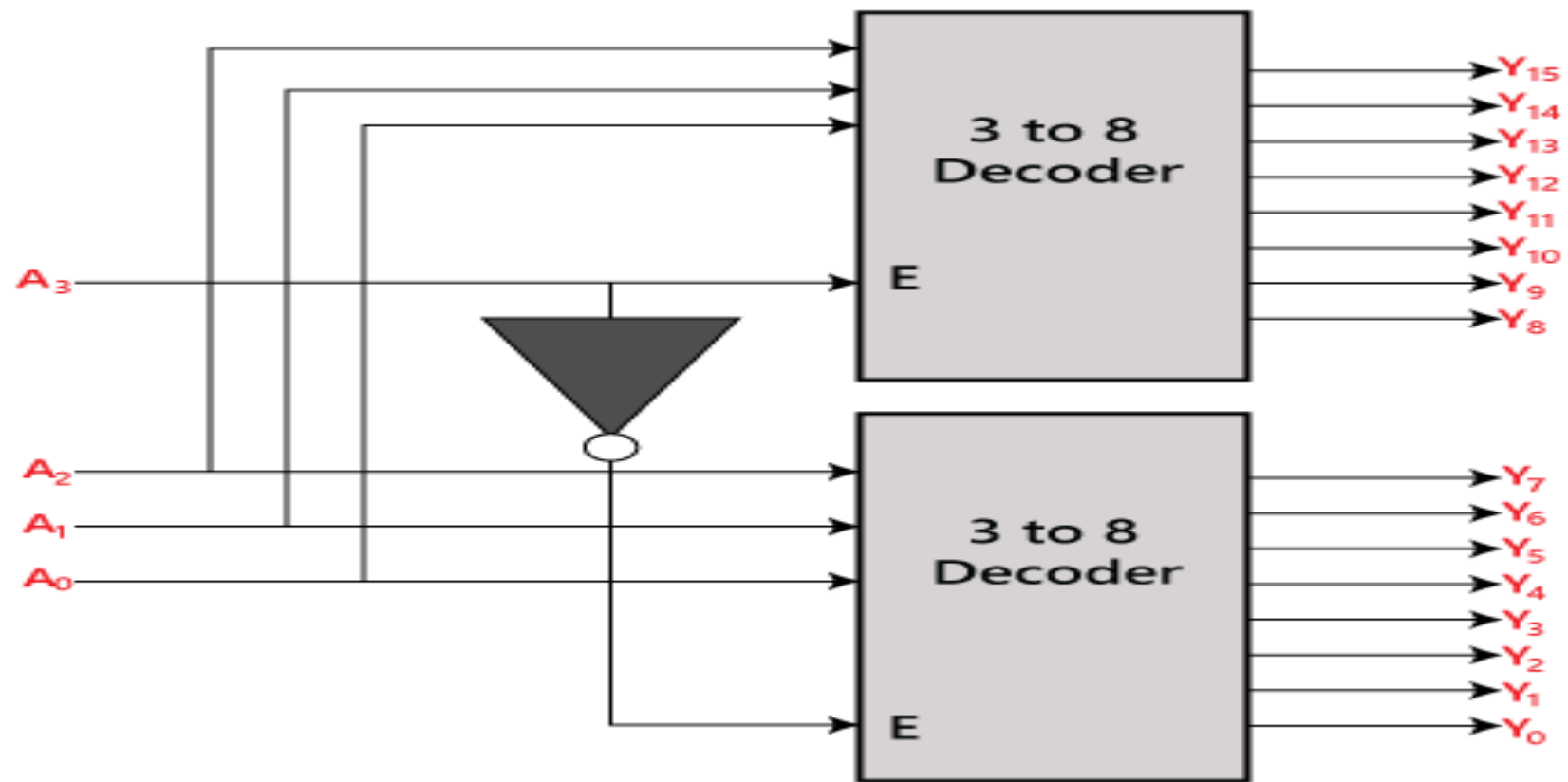
There is the following formula used to find the required number of lower-order decoders.

Required number of lower order decoders = m_2/m_1

$$m_1 = 8$$

$$m_2 = 16$$

Required number of 3 to 8 decoders = $\quad = 2$



- The logical expression of the term $A_0, A_1, A_2, \dots, A_{15}$ are as follows:

- $Y_0 = A_0' \cdot A_1' \cdot A_2' \cdot A_3'$
- $Y_1 = A_0' \cdot A_1' \cdot A_2' \cdot A_3$
- $Y_2 = A_0' \cdot A_1' \cdot A_2 \cdot A_3'$
- $Y_3 = A_0' \cdot A_1' \cdot A_2 \cdot A_3$
- $Y_4 = A_0' \cdot A_1 \cdot A_2' \cdot A_3'$
- $Y_5 = A_0' \cdot A_1 \cdot A_2' \cdot A_3$
- $Y_6 = A_0' \cdot A_1 \cdot A_2 \cdot A_3'$
- $Y_7 = A_0' \cdot A_1 \cdot A_2 \cdot A_3$
- $Y_8 = A_0 \cdot A_1' \cdot A_2' \cdot A_3'$
- $Y_9 = A_0 \cdot A_1' \cdot A_2' \cdot A_3$
- $Y_{10} = A_0 \cdot A_1' \cdot A_2 \cdot A_3'$
- $Y_{11} = A_0 \cdot A_1' \cdot A_2 \cdot A_3$
- $Y_{12} = A_0 \cdot A_1 \cdot A_2' \cdot A_3'$
- $Y_{13} = A_0 \cdot A_1 \cdot A_2' \cdot A_3$
- $Y_{14} = A_0 \cdot A_1 \cdot A_2 \cdot A_3'$
- $Y_{15} = A_0 \cdot A_1 \cdot A_2 \cdot A_3$

