Electronics

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Basic comparator

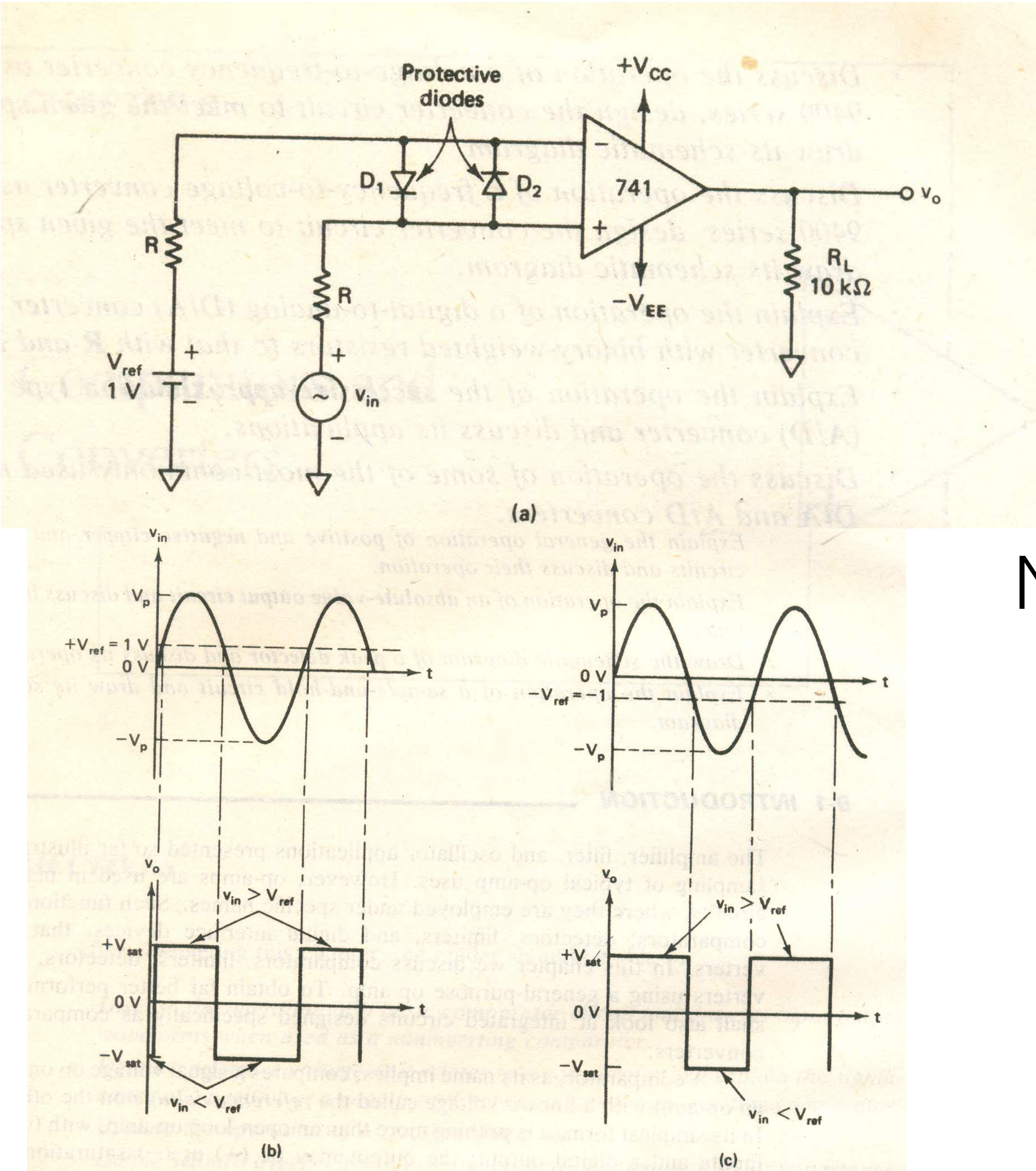


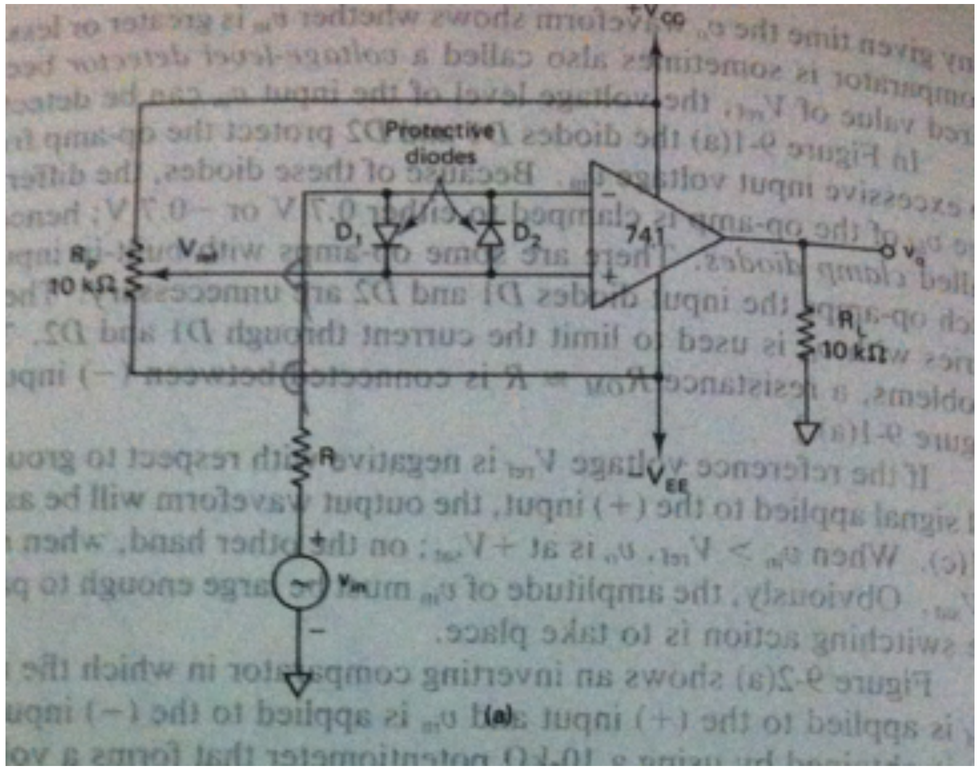
Figure 9–1 (a) Noninverting comparator and its input and output waveforms. (b) If V_{ref} is positive. (c) If V_{ref} is negative.

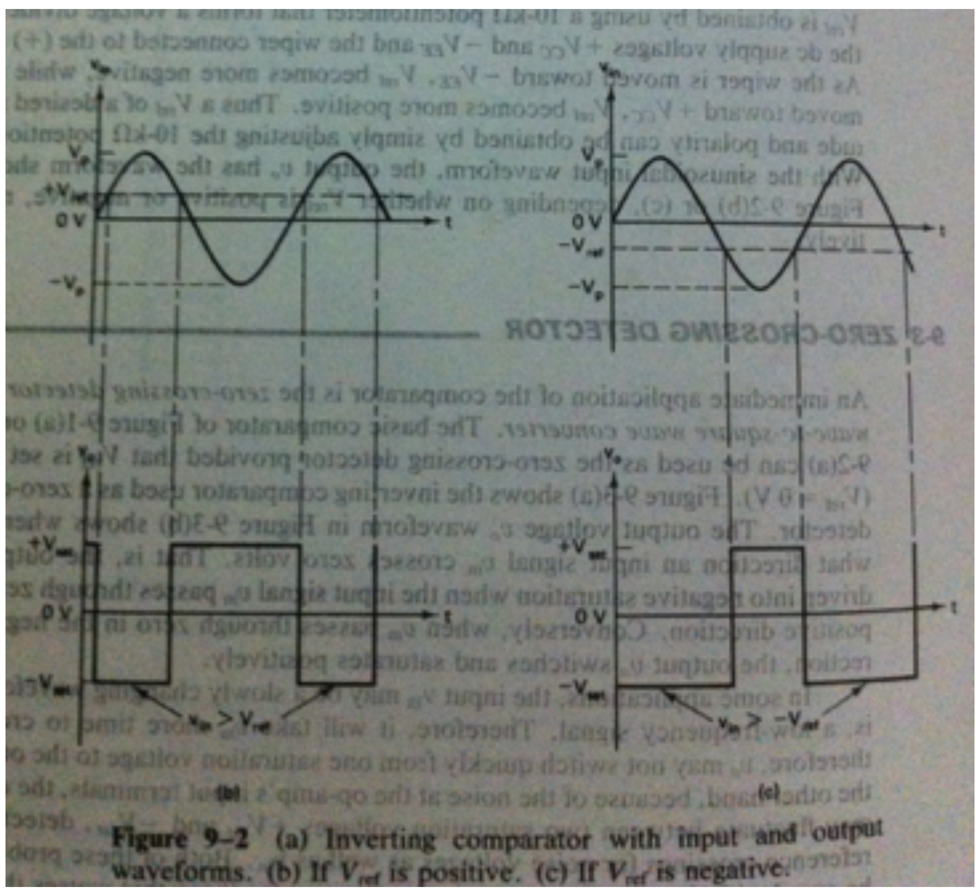
Noninverting comparator

A fixed reference voltage Vref = 1V is applied at (-) input and a time varying voltage Vin is applied at (+) input. It is also called Noninverting comparator

When vin is less than Vref the output voltage V0 = Vsat (-VEE) and When vin is greater than Vref the output voltage V0 = Vsat (+Vcc)

The diodes D1 and D2 are called clamp diodes They protect the opamp from damage due to excessive input voltage Vin. Because of these diodes the input difference voltage is clamped to either 0.7 or -0.7 V.





Inverting comparator

A fixed reference voltage Vref is applied at (+) input and a time varying voltage Vin is applied at (-) input. It is also called inverting comparator

Application of the comparator
Zero crossing detector

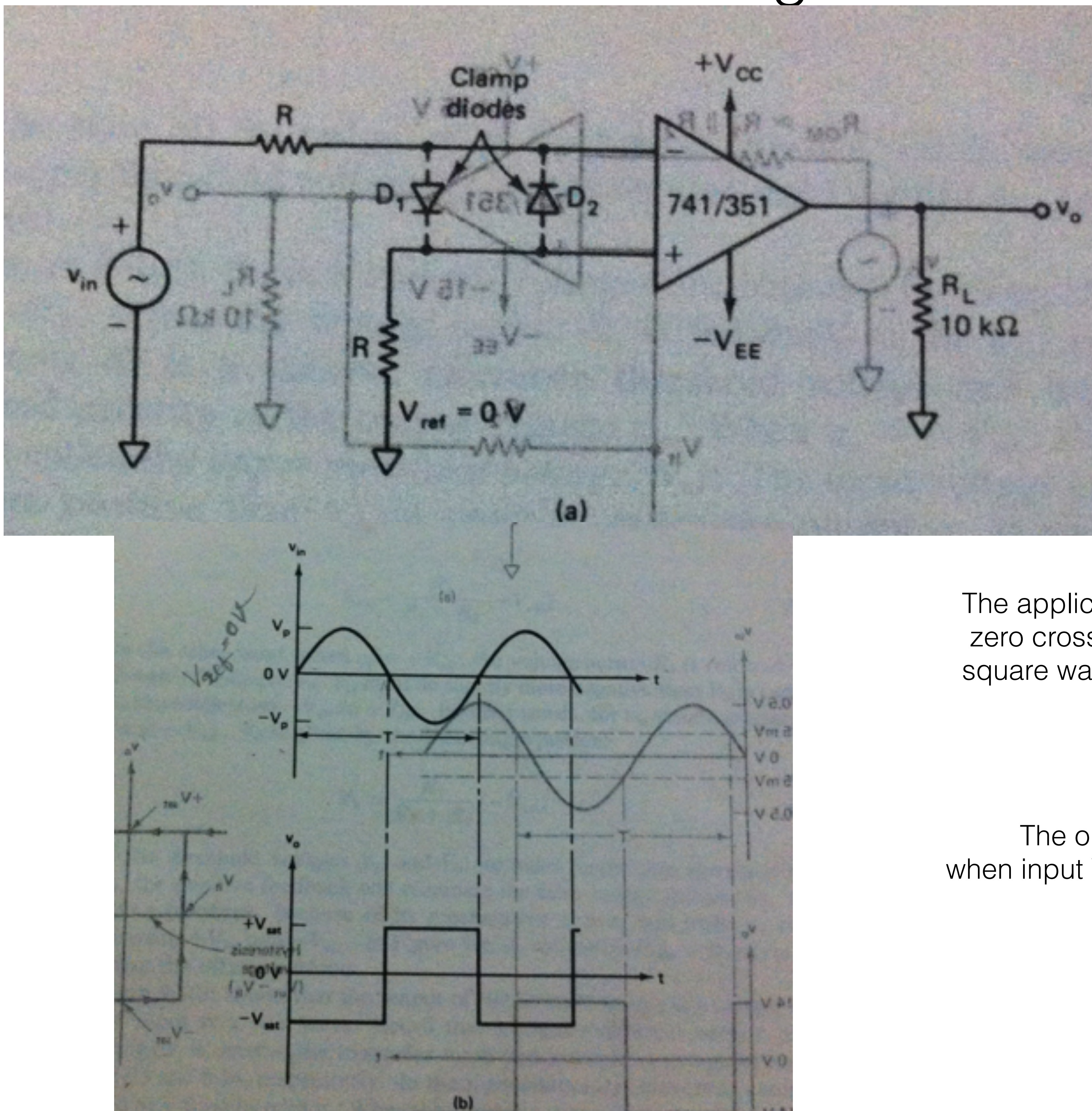
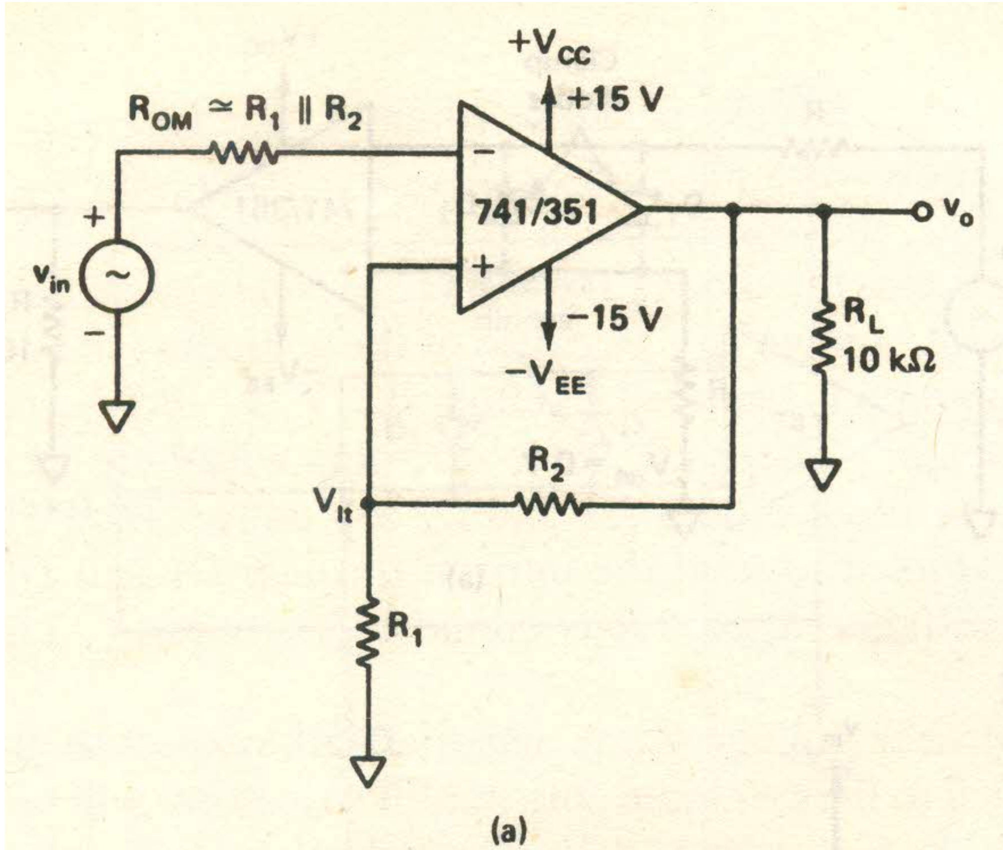


Figure 9–3 (a) Zero-crossing detector. (b) Its typical input and output waveforms.

The application of the comparator is a zero crossing detector or a sine wave to square wave converter. here Vref is set to 0V

The output V0 is driven to negative saturation when input Vin crosses zero volts in the positive direction

Schmitt Trigger



The circuit converts an irregular shaped waveform to a square wave or pulse.
The input voltage vin triggers the output v0 every time it exceeds certain voltage levels called upper threshold voltage Vut and lower threshold voltage Vlt.

$$V_{ut} = \frac{R_1}{R_1 + R_2}(+V_{sat})$$

$$V_{lt} = \frac{R_1}{R_1 + R_2}(-V_{sat})$$

$$V_{hy} = V_{ut} - V_{lt}$$
$$= \frac{R_1}{R_1 + R_2}[+V_{sat} - (-V_{at})]$$

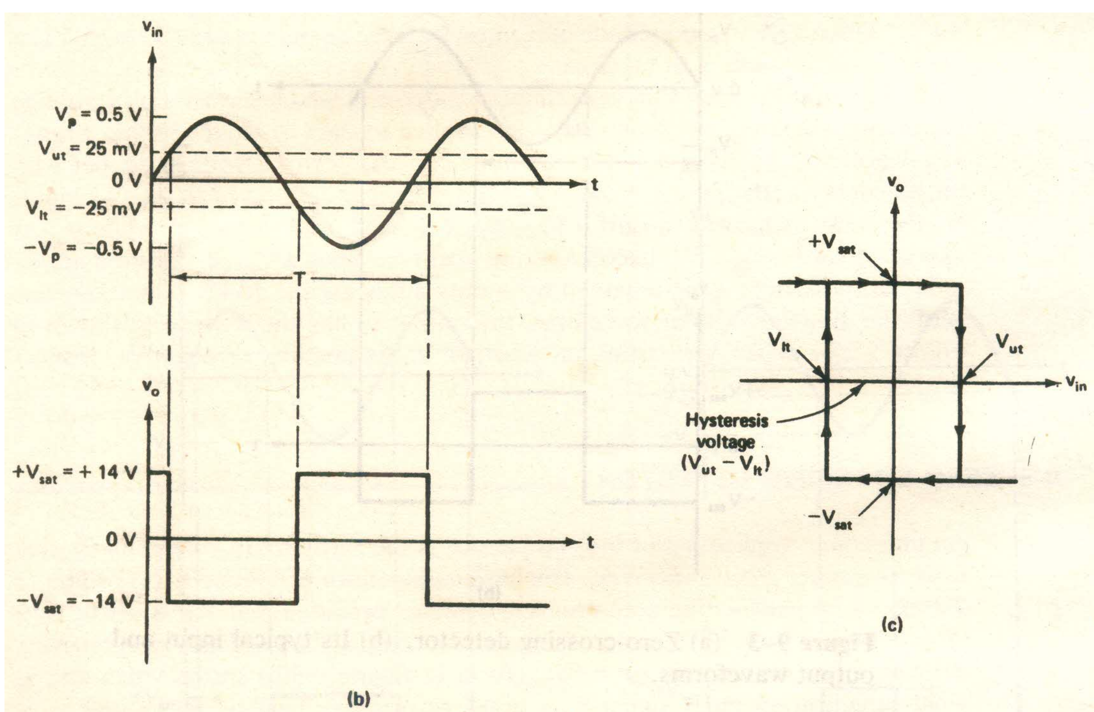
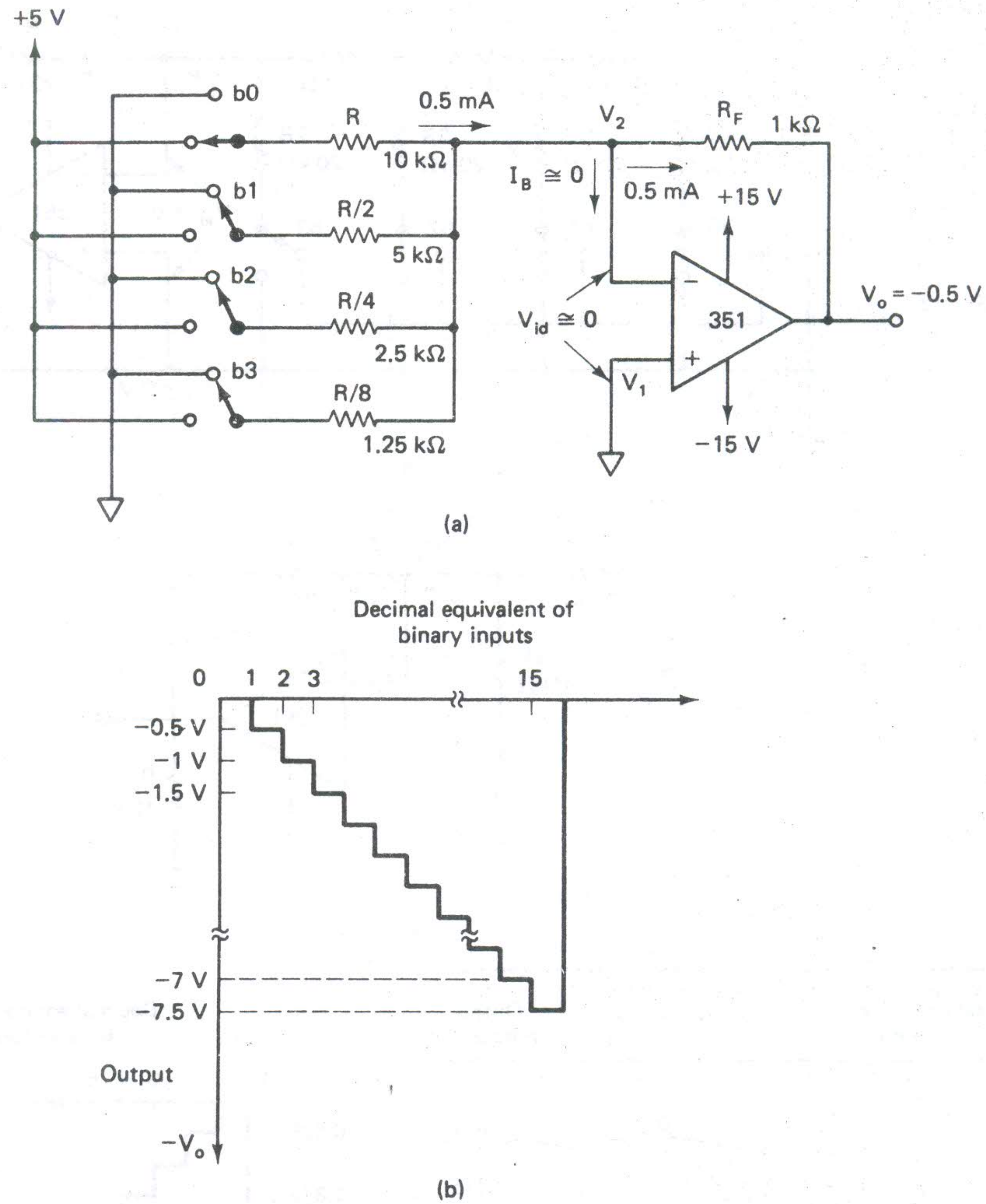


Figure 9–4 (a) Inverting comparator as Schmitt trigger. (b) Input and output waveforms of Schmitt trigger. (c) v_o versus v_{in} plot of the hysteresis voltage.

Digital to Analog converter

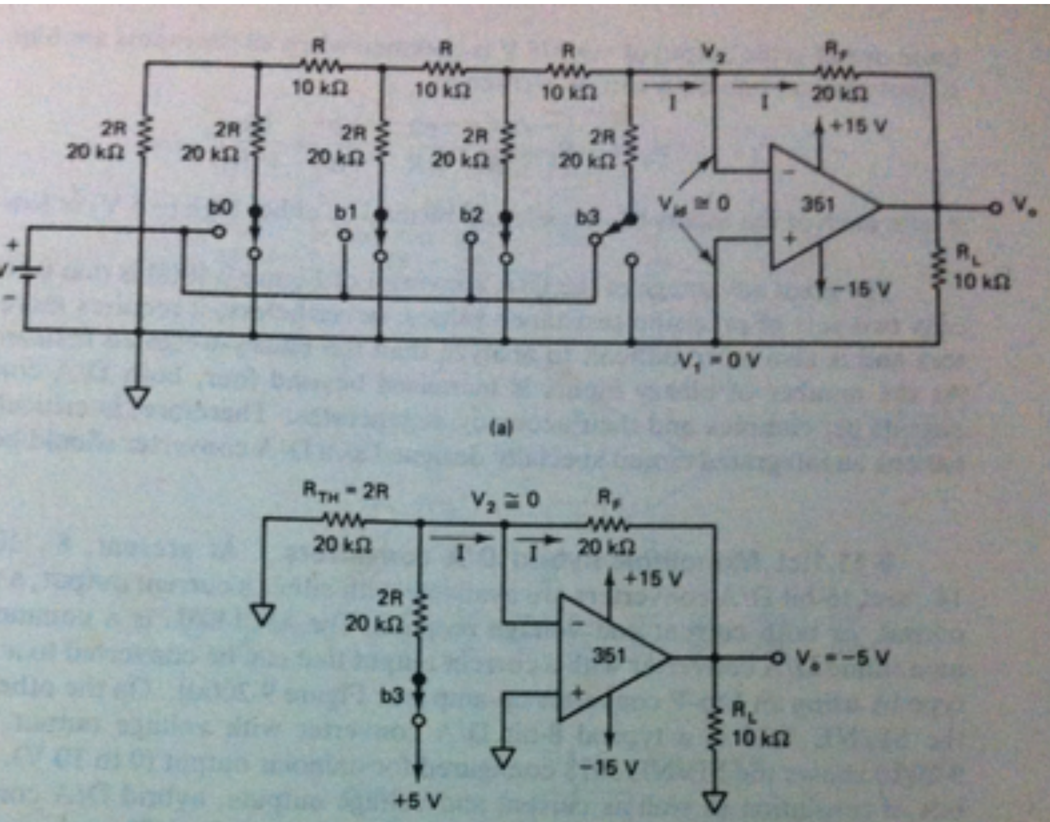
binary weighted resisters



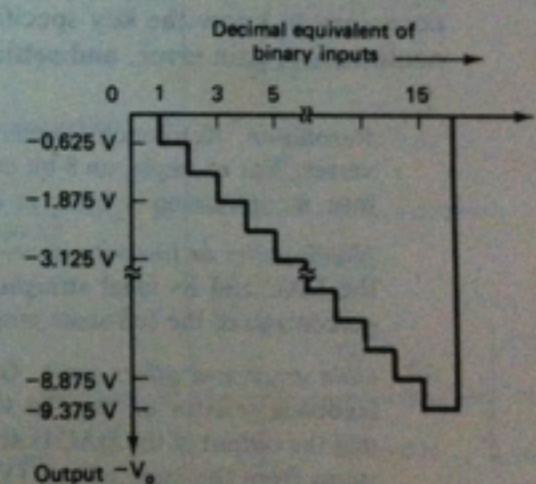
GURE 8–18 (a) D/A converter with binary-weighted resistors. (b) Graph of output
sus inputs.

A D/A converter uses an opamp and either binary weighted resisters or R and 2R resisters.

R and 2R resisters



Decimal equivalent of binary inputs	Input (V) b3	b2	b1	b0	Output voltage (V)
0	0	0	0	0	0
1	0	0	0	5	−0.625
2	0	0	5	0	−1.25
3	0	0	5	5	−1.875
4	0	5	0	0	−2.50
5	0	5	0	5	−3.125
6	0	5	5	0	−3.750
7	0	5	5	5	−4.375
8	5	0	0	0	−5.0
9	5	0	0	5	−5.625
10	5	0	5	0	−6.25
11	5	0	5	5	−6.875
12	5	5	0	0	−7.50
13	5	5	0	5	−8.125
14	5	5	5	0	−8.875
15	5	5	5	5	−9.375



(c)

Figure 9–19 (a) D/A converter with *R*/2*R* resistors. (b) Equivalent circuit when b3 is high and b0, b1, and b2 are low. (c) Output versus inputs.

Analog to digital converter (A/D)

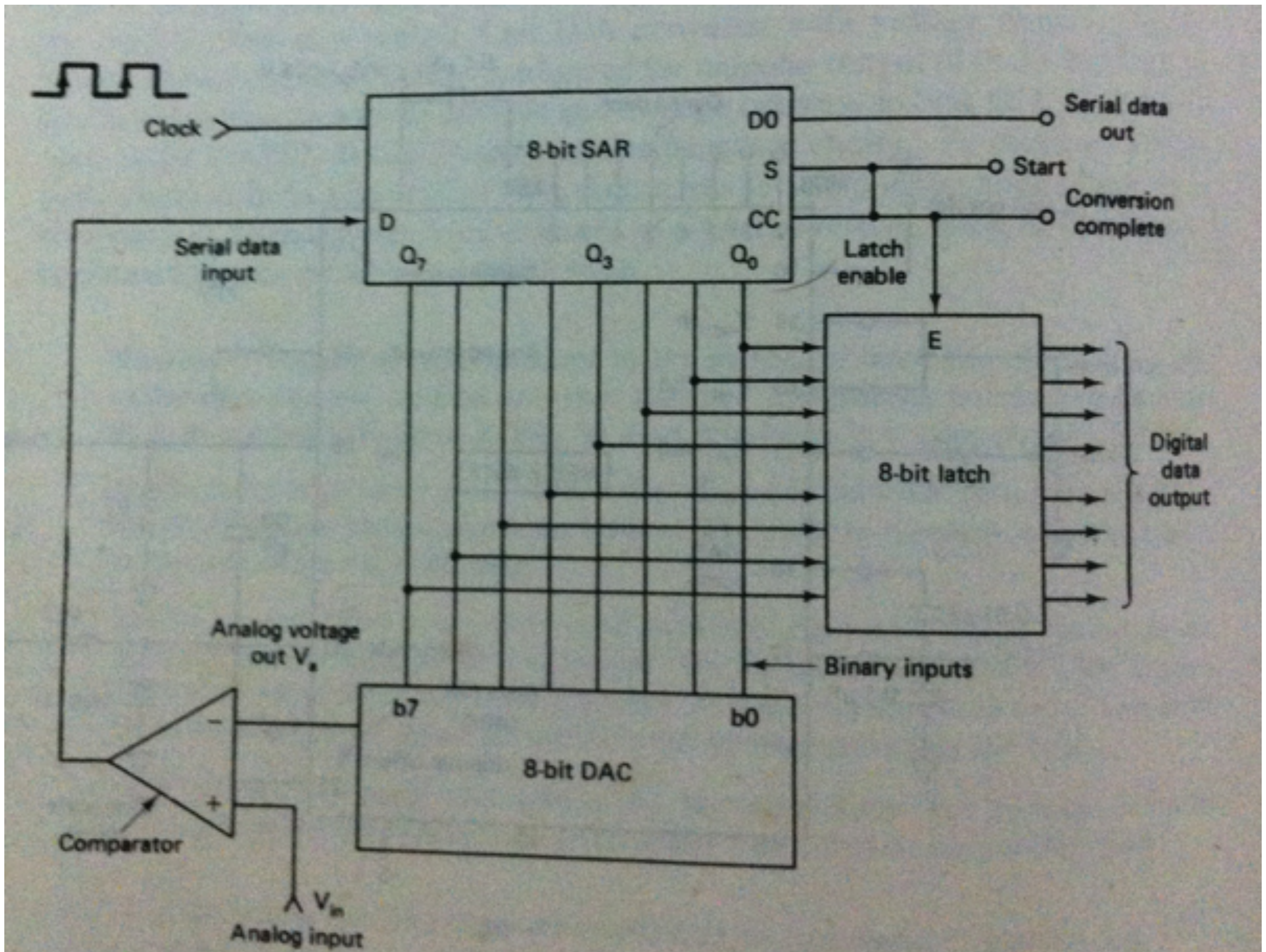


Figure 9–21 Successive-approximation-type A/D converter.

Peak Detector

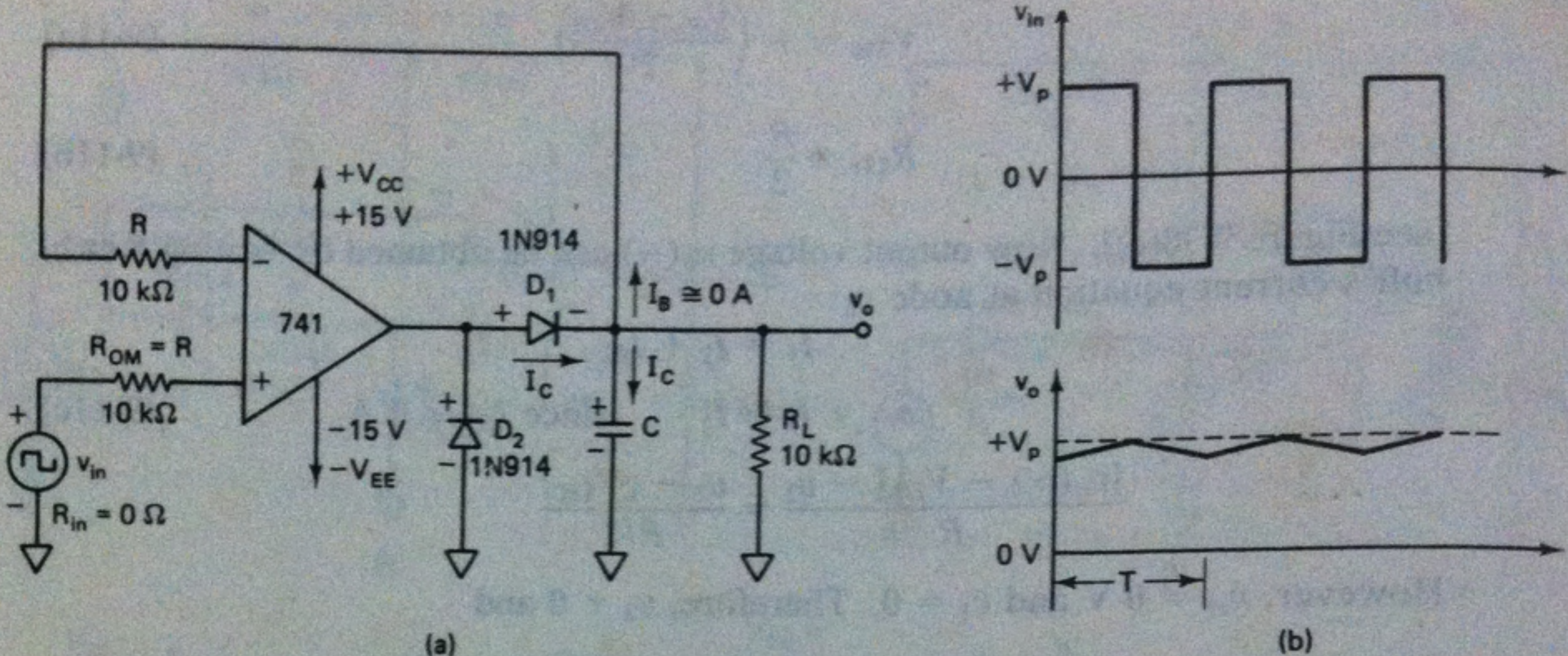


Figure 9–31 (a) Peak detector circuit. (b) Its input and output waveforms.

Sample and hold circuit

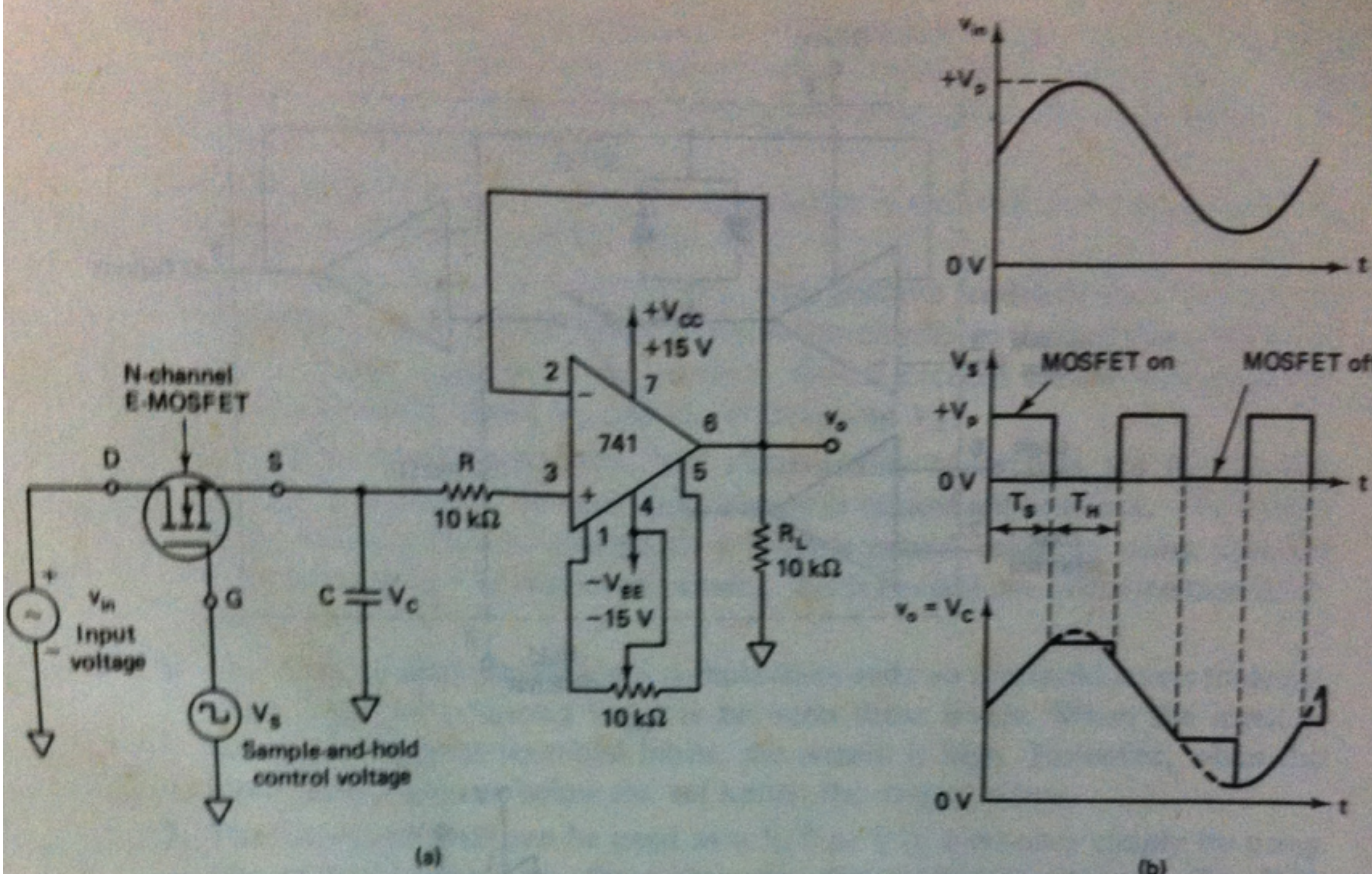


Figure 9–32 (a) Sample-and-hold circuit. (b) Its input and output waveforms.

IC555 timer internal architecture

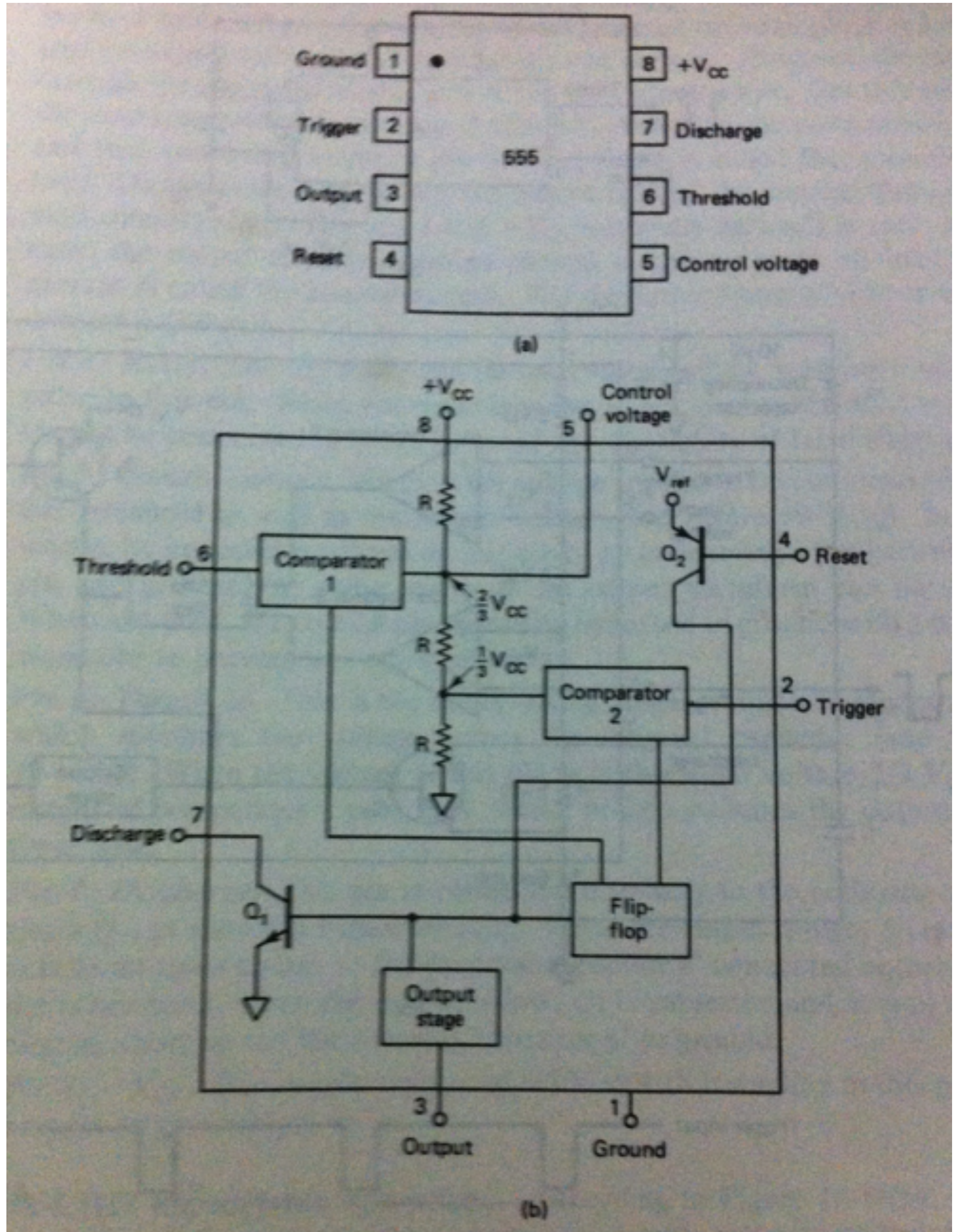
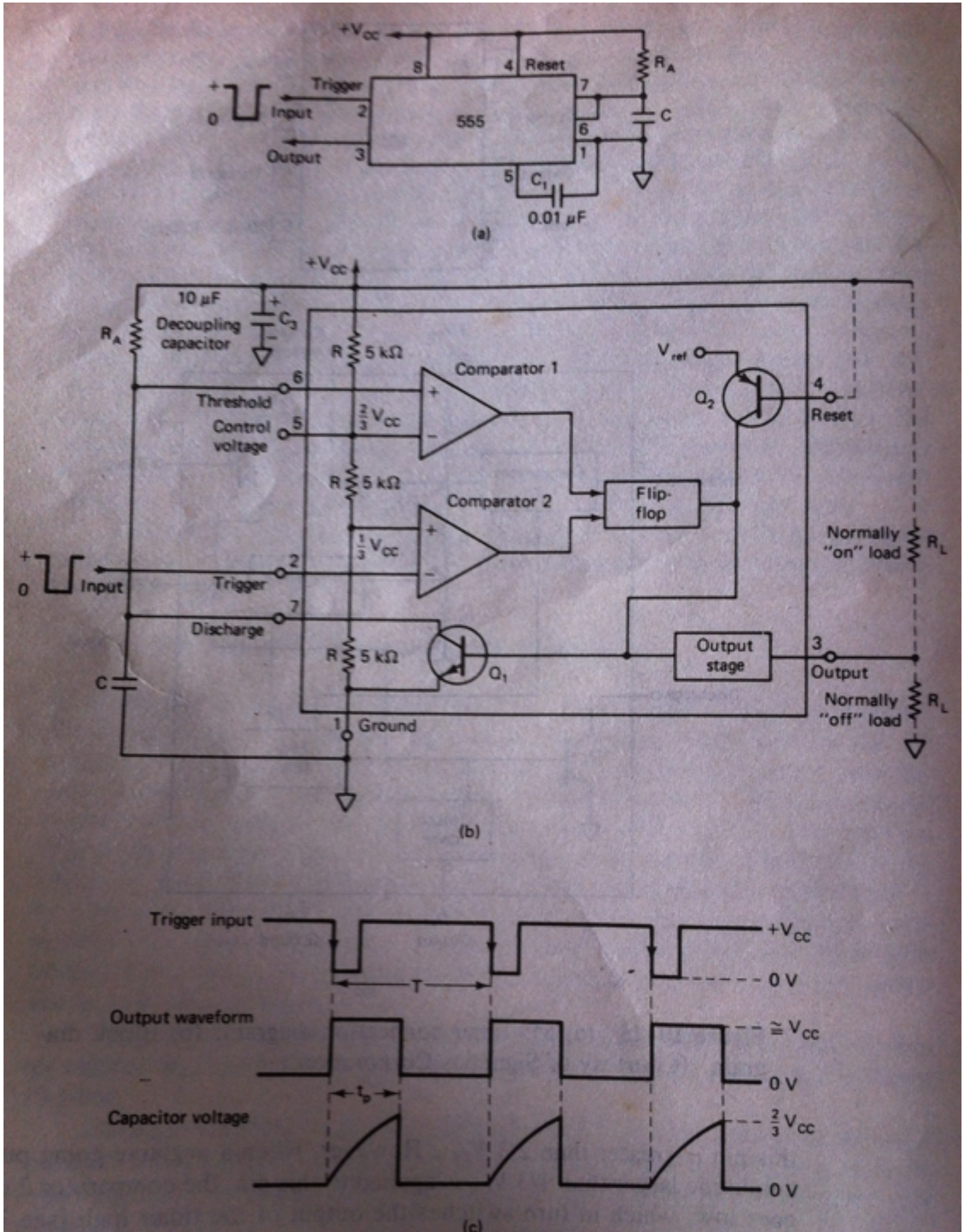


Figure 10–15 (a) 555 timer connection diagram. (b) Block dia-


+Vcc
8
4 Reset
RA
Trigger
Input
2
7
555
C
6
Output
3
1
5
C1
0.01 μF
(a)
+Vcc
10 μF
Decoupling capacitor
C3
RA
R 5 kΩ
Vref
Comparator 1
6
Threshold
2/3 Vcc
Q2
4
Reset
Control voltage
5
R 5 kΩ
Comparator 2
Flip-flop
1/3 Vcc
Normally "on" load
RL
Input
2
Trigger
7
Discharge
R 5 kΩ
Q1
Output stage
3
Output
C
Normally "off" load
RL
1
Ground
(b)
Trigger input
+Vcc
T
0 V
Output waveform
≅ Vcc
0 V
tp
Capacitor voltage
2/3 Vcc
0 V
(c)

Phase Locked Loop

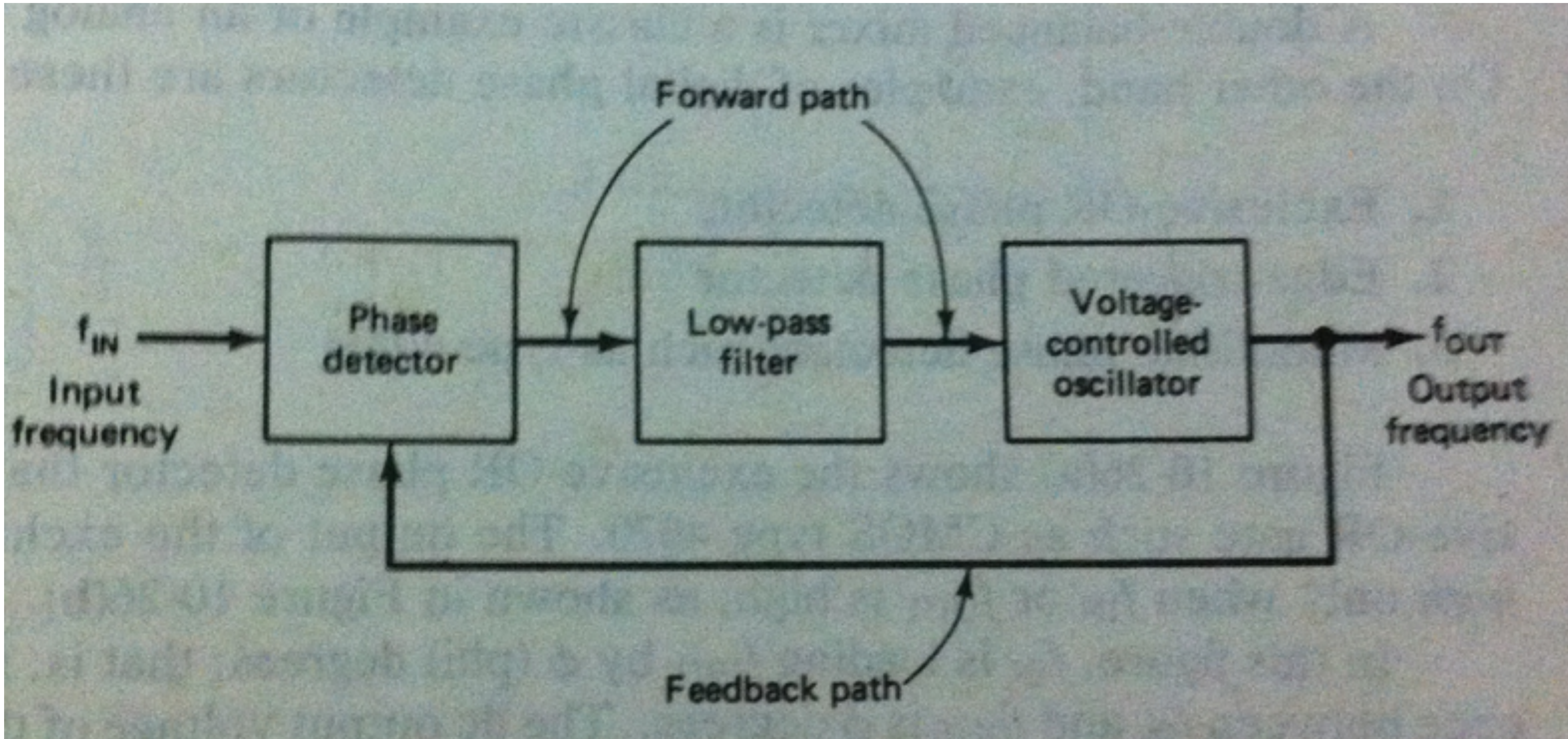


Figure 10–25 Block diagram of a phase-locked loop.

Applications IC565 - PLL Frequency Multiplier

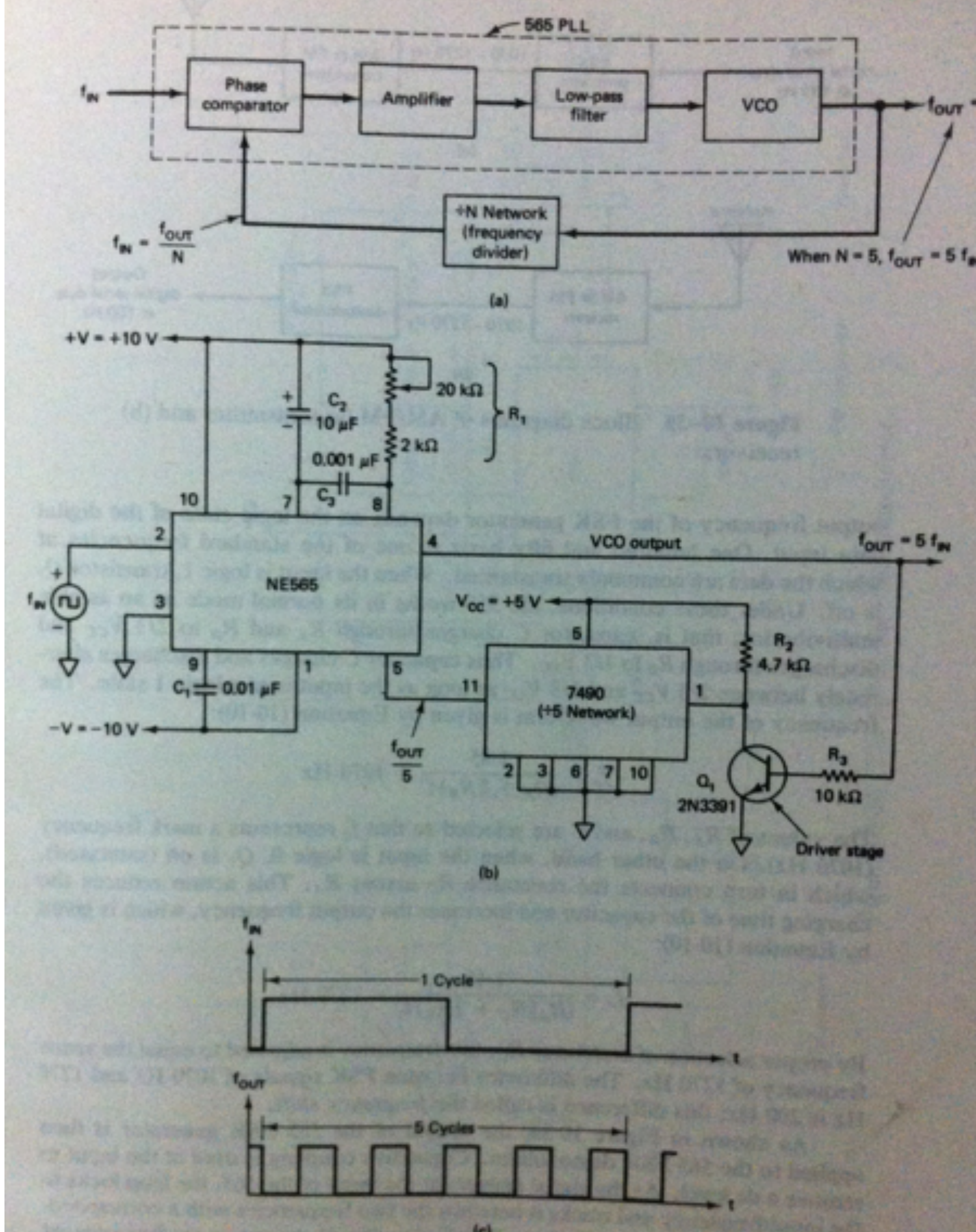


Figure 10–34 Frequency multiplier using the 565. (a) Block diagram. (b) Connection diagram for multiply-by-5. (c) Input–output waveforms.