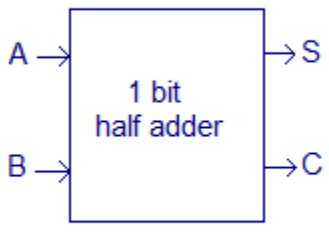
COMBINATIONAL LOGIC

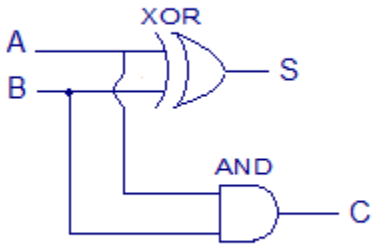
Half-Adder

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Truth table



Schematic



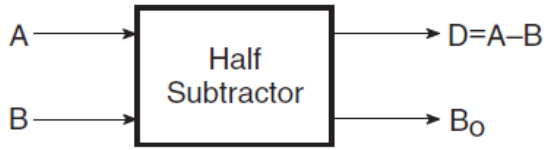
Realization

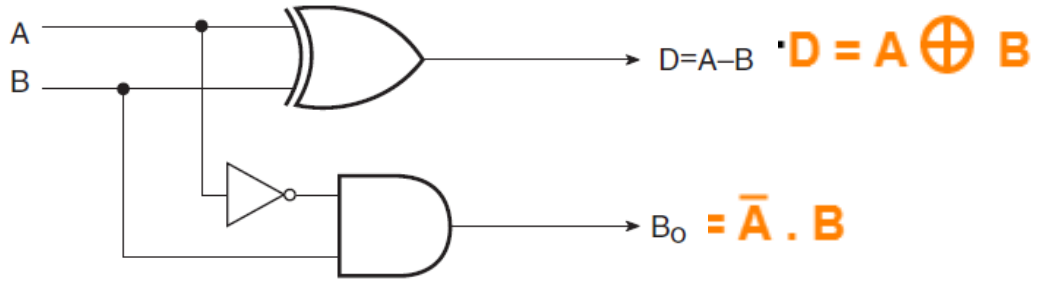
SUM
$A \oplus B$

CARRY
$A \cdot B$

Half-Subtractor

A	B	D	B_O
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0





Full-Adder

Inputs			Outputs	
A	B	C_{in}	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 3.7 Truth table for full-adder

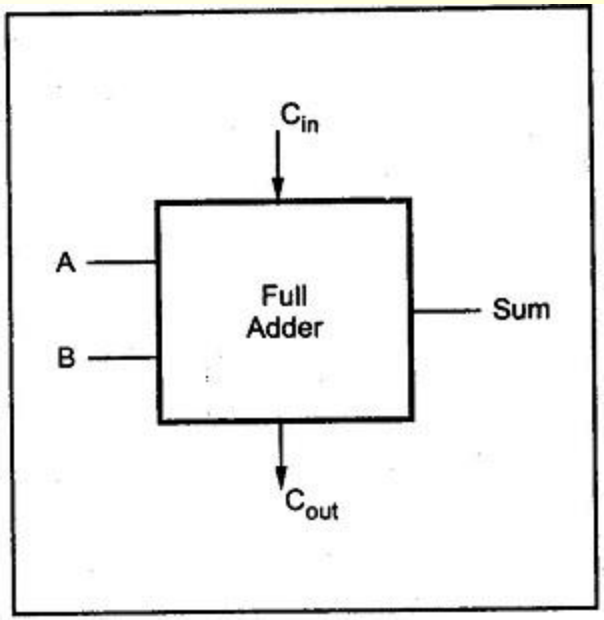


Fig. 3.14 Block schematic of full-adder

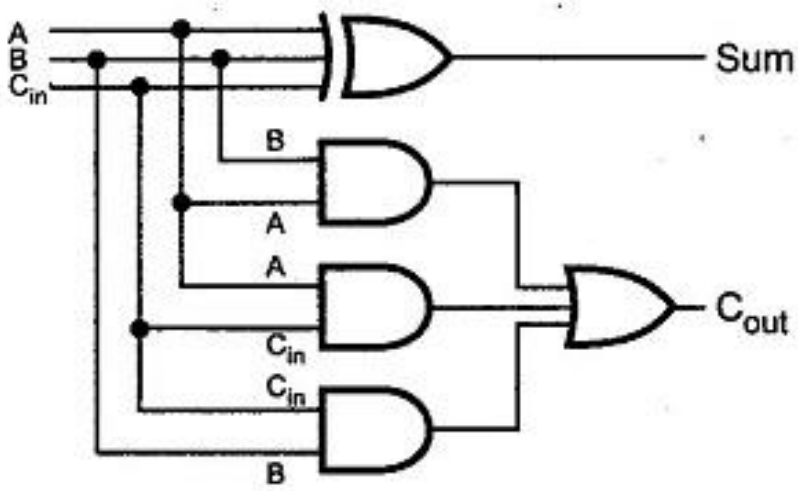
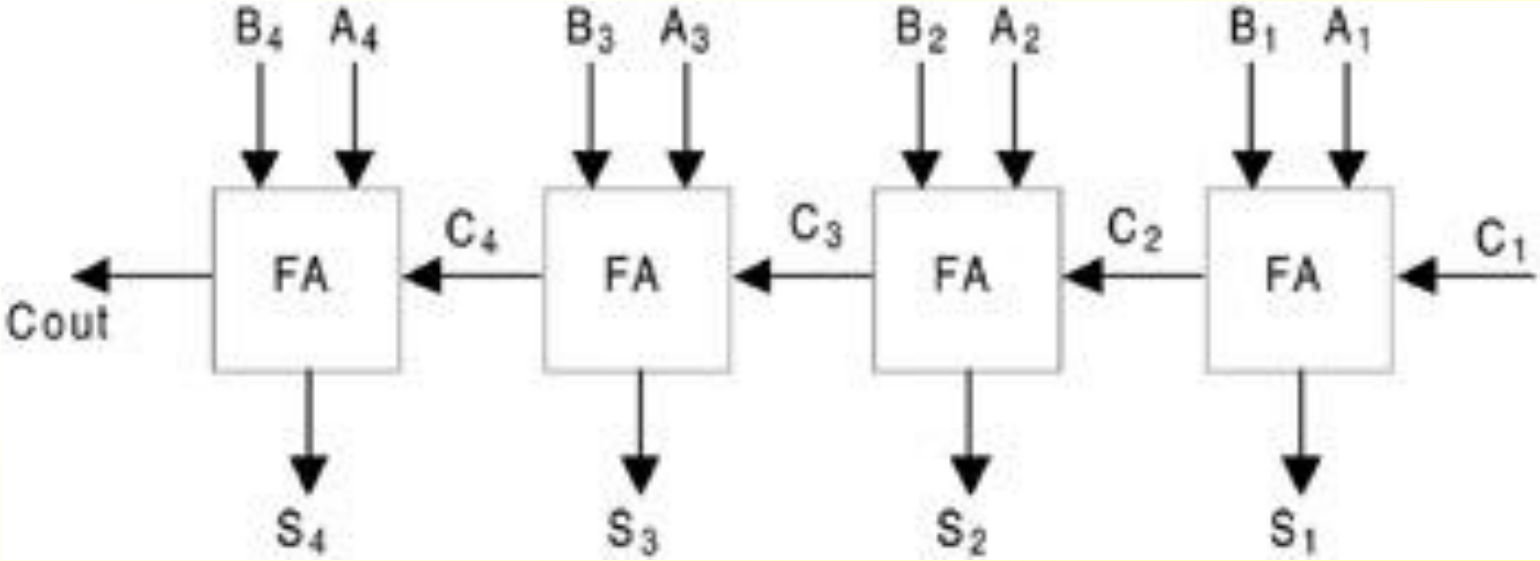


Fig. 3.17 Implementation of full-adder

$$S = A \oplus B \oplus C_{in}$$

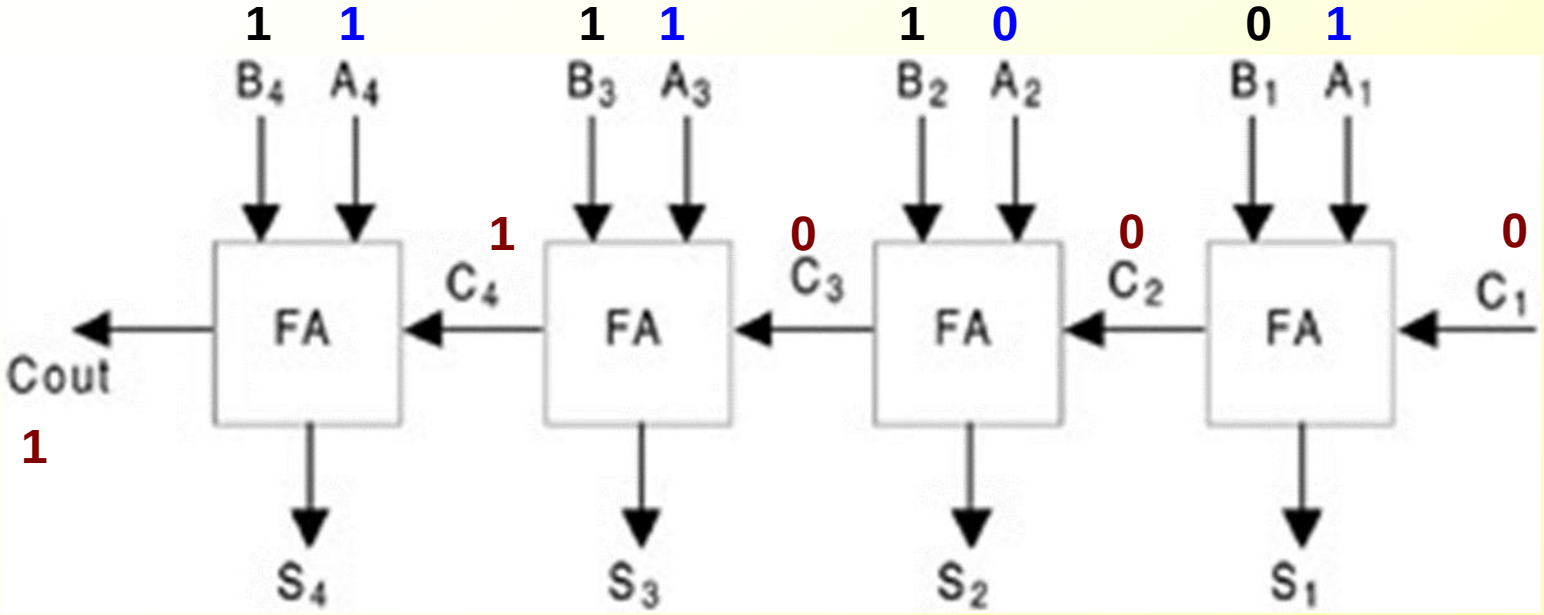
$$C_{out} = AB + BC_{in} + C_{in}A$$

Four bit adder



- ✓ In practical situations, it is required to add two data each containing four bits. This can be done by cascading four full adder circuits as shown in figure.

- ✓ **Working:** Suppose we want to add two 4-bit binary numbers $B_4B_3B_2B_1$ and $A_4A_3A_2A_1$ with a carry input C_1.The least significant bits A_1, B_1, and C_1 are added to the produce sum output S_1 and carry output C_2. Carry output C_2 is then added to the next significant bits A_2 and B_2 producing sum output S_2 and carry output C_3. Then C_3 is added to A_3 and B_3 and so on. Thus finally producing the four-bit sum output $S_4S_3S_2S_1$ and final carry output Cout.

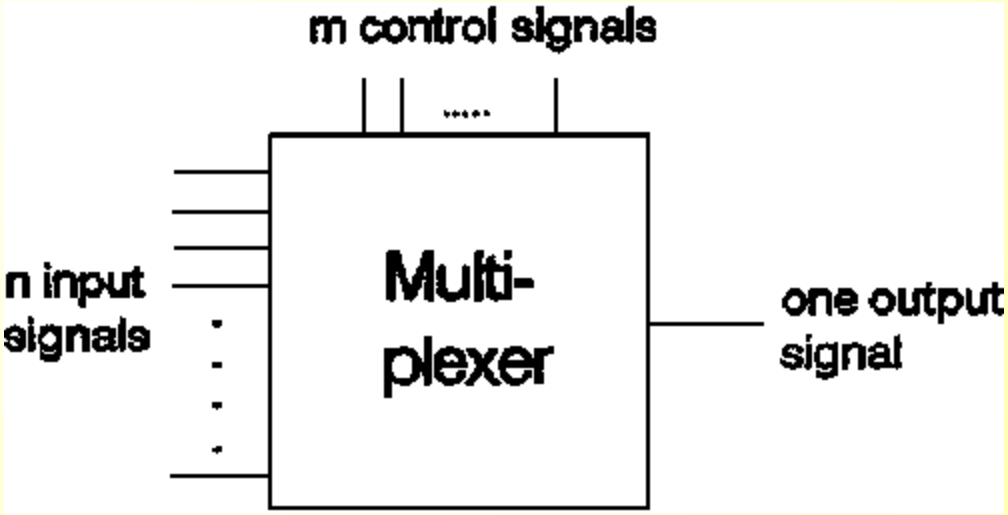


For Example,

1 0 0 0	$C_4C_3C_2C_1$
1101	$A_4A_3A_2A_1$
+1110	$B_4B_3B_2B_1$
1011	$S_4S_3S_2S_1$
With a carry 1	With a carry Cout =1

Thus for adding two four-bit numbers, we need four Full adders and hence for adding two n-bit numbers, we need n full adder circuits

Multiplexers



Multiplexer means *many into one.* By applying control signals, we can steer any input to the output.

16-to-1 Multiplexer (Data Selector)

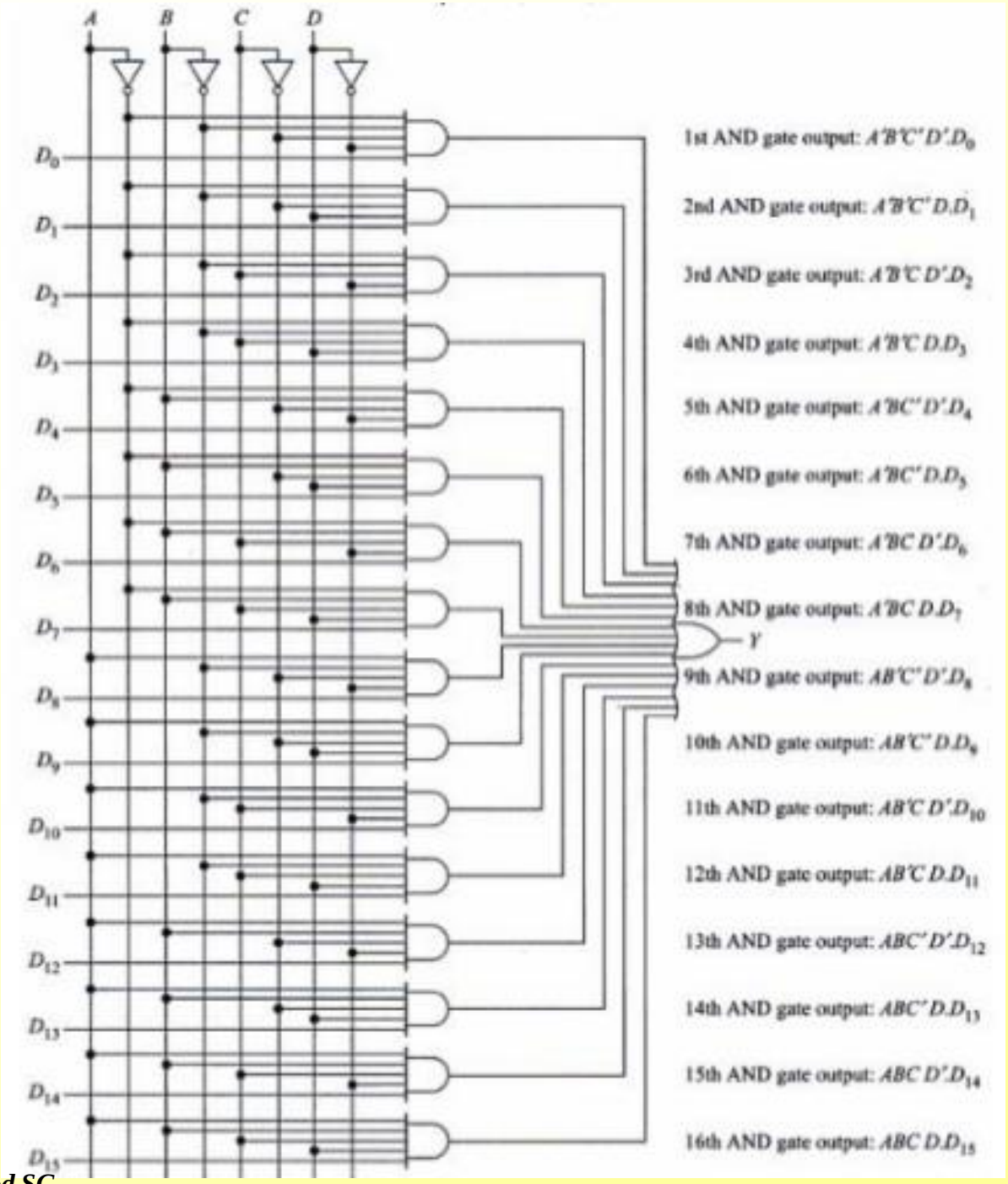
✓Here one of the inputs is transmitted to o/p which depends on the value of ABCD.

✓When ABCD=0000, upper AND gate is enabled and D_0 is transmitted to the o/p.

✓Similarly, when ABCD=1111, all AND gates are disabled except the bottom one, so that $Y=D_{15}$.

✓For 2^n data input lines, there will be *n* selection lines, and always a *single* output line.

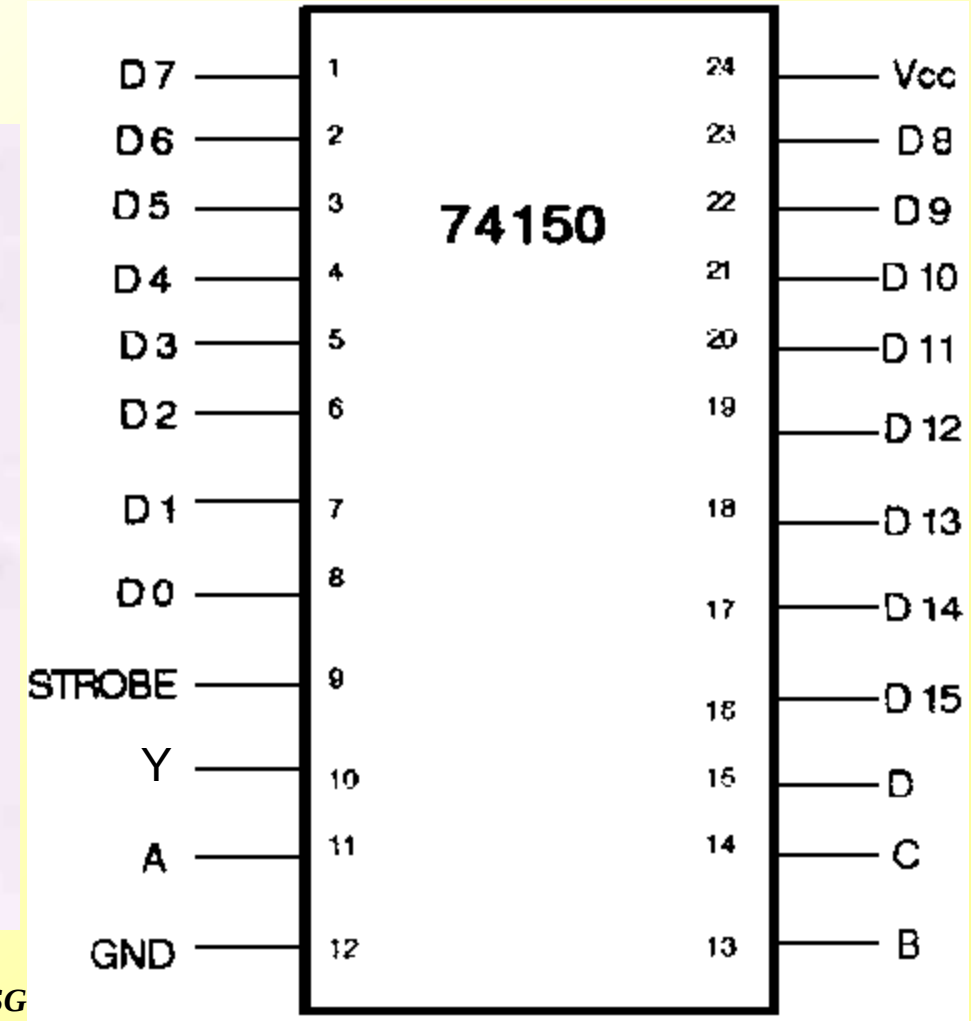
For example, for an *8-to-1 Multiplexer*, there are 8 input lines and 3 control lines. Similarly for an *4-to-1 Multiplexer,* there are 4 input lines and 2 control lines and so on.



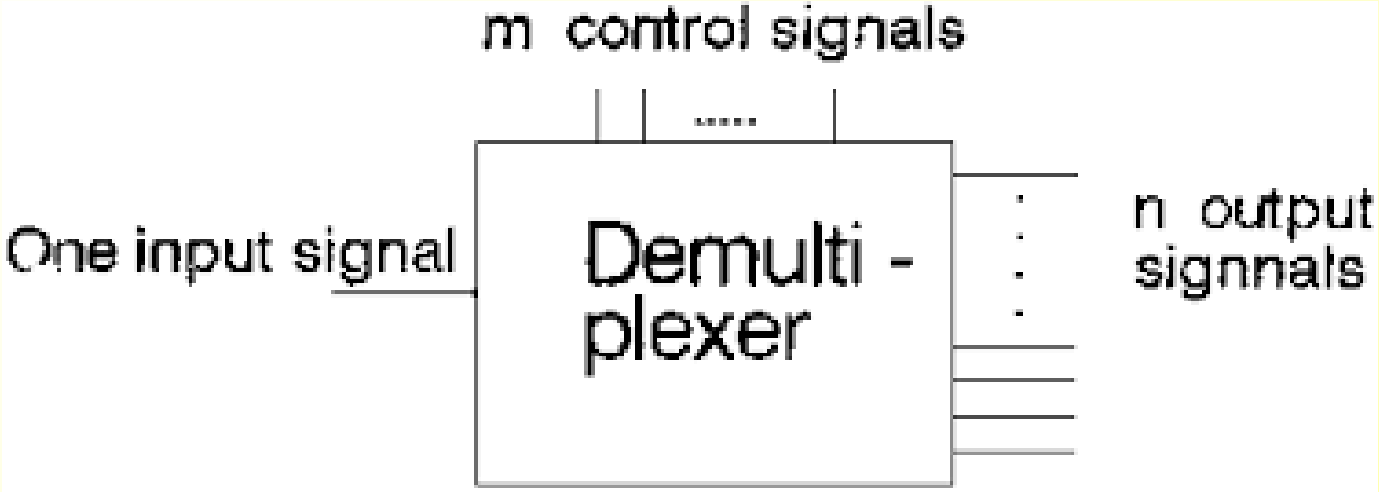
IC 74150-Multiplexer

- Here 16-input OR gate is changed to a NOR gate. So we get the complement of the selected data bit. For instance, when ABCD=0111, the output is $Y=\overline{D}_7$.
- Pin 1 to 8 and 16 to 23 are for the input data bits D_0 to D_{15}.Pins 11,13,14 and 15 are for the control bits ABCD. Pin 10 is the output, and is equal to the complement of the selected data input. Pin 9 is STROBE, an input signal that disables or enables the multiplexer

Strobe	A B C D	Y
L	L L L L	$\overline{D}_0$
L	L L L H	$\overline{D}_1$
L	L L H L	$\overline{D}_2$
L	L L H H	$\overline{D}_3$
L	L H L L	$\overline{D}_4$
L	L H L H	$\overline{D}_5$
L	L H H L	$\overline{D}_6$
L	L H H H	$\overline{D}_7$
L	H L L L	$\overline{D}_8$
L	H L L H	$\overline{D}_9$
L	H L H L	$\overline{D}_{10}$
L	H L H H	$\overline{D}_{11}$
L	H H L L	$\overline{D}_{12}$
L	H H L H	$\overline{D}_{13}$
L	H H H L	$\overline{D}_{14}$
L	H H H H	$\overline{D}_{15}$
H	X X X X	H



Demultiplexers



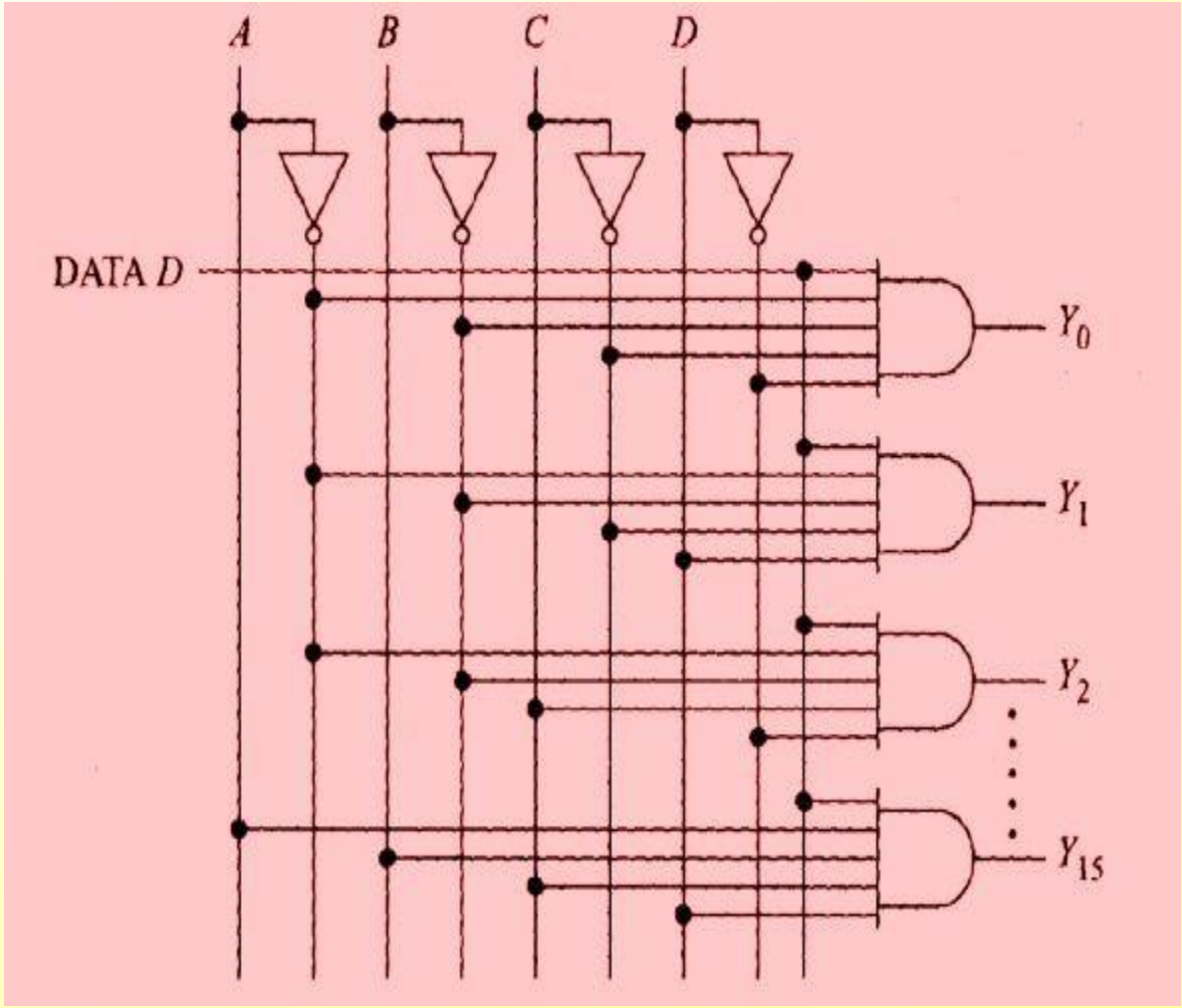
Demultiplexer means *one into many.* By applying control signals, we can steer the input signal to one of the output lines.

1-to-16 demultiplexer

✓Here the input bit D is transmitted to one of the o/p lines, which depends on the value of ABCD.

✓When ABCD=0000, upper AND gate is enabled, while all others are disabled and D is transmitted only to the Y_0 o/p, giving Y_0=D.

✓Similarly, when ABCD=1111, all AND gates are disabled except the bottom one, so that Y_{15}=D.



IC 74154-Demultiplexer

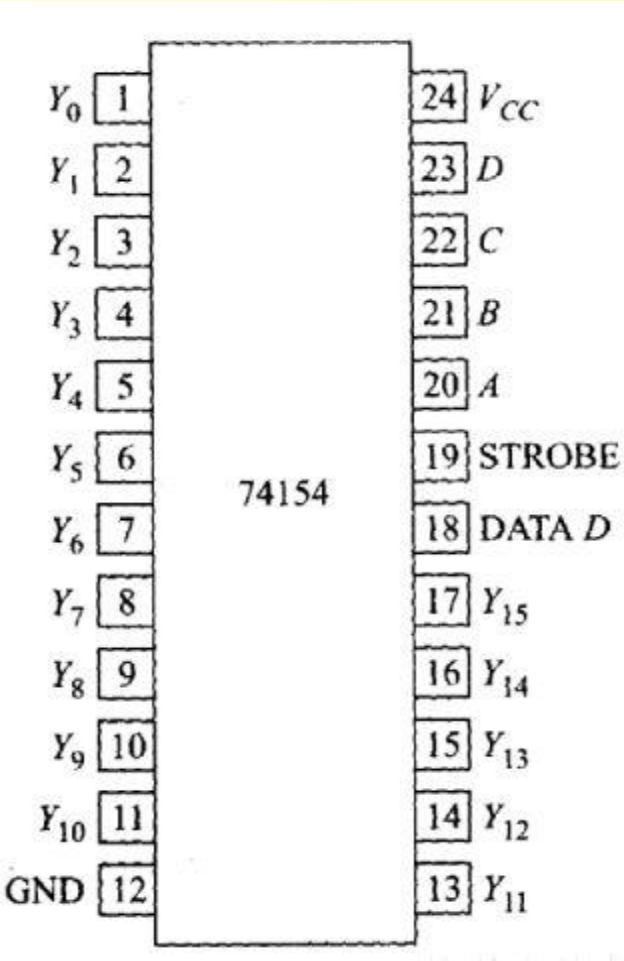
Here pin 18 is the input data D, and pins 20 to 23 are control bits ABCD. Pins 1 to 11 and 13 to 17 are for the outputs Y_0 to Y_{15}

Pin 19 is STROBE, an input signal that disables or enables the demultiplexer.

When STROBE is low, the control input ABCD determines which of the output lines is low, when the data input is low.

STROBE has to be low, to activate the IC. When it is high, all the o/ps are high.

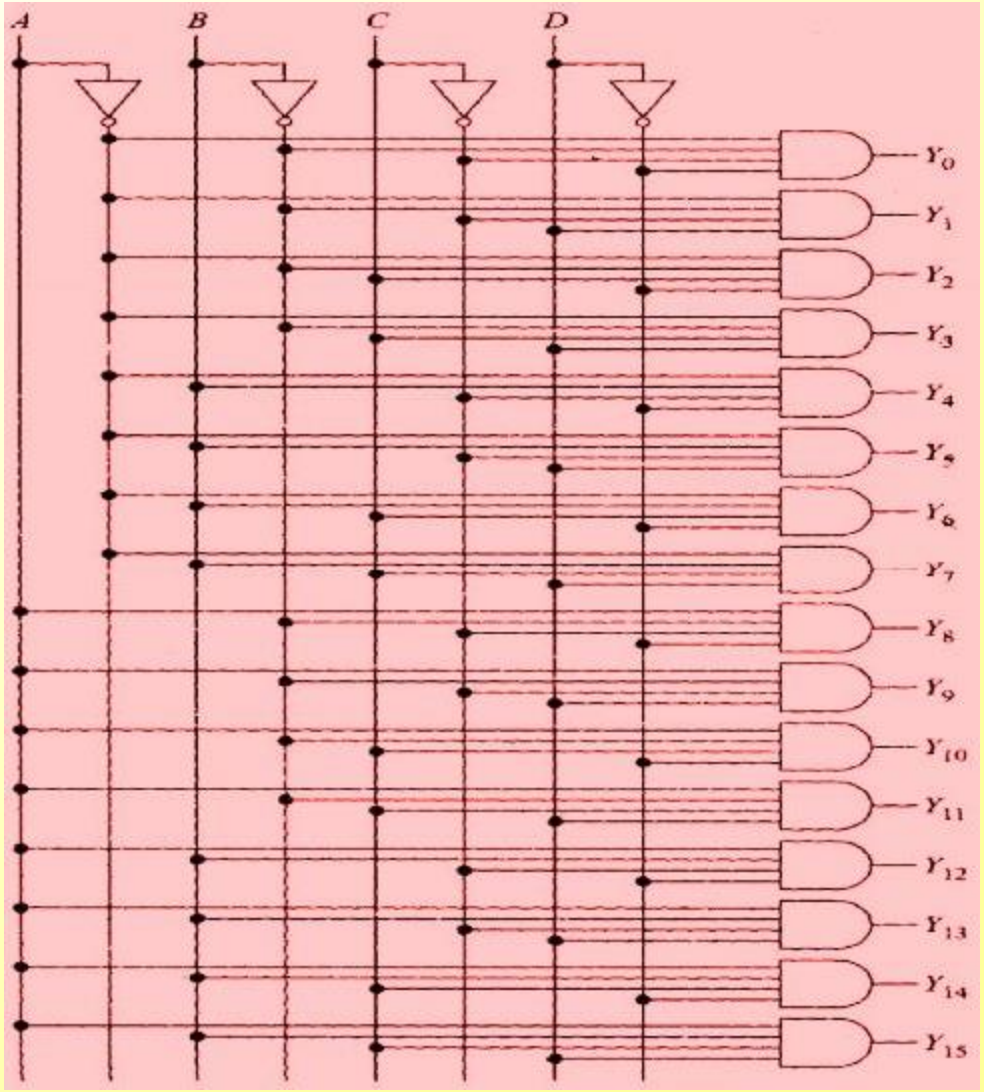
Strobe	Data	A	B	C	D	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H



1-of-16 decoder

A Decoder is similar to a demultiplexer, with one exception-there is no data input. The only inputs are the control bits ABCD as shown in figure.

- ✓**The logic circuit is called 1-of-16 decoder because only 1 of the 16 output lines is high**
- ✓**For instance, when ABCD is 0001, only the Y_1 AND gate has all inputs high; as a result, only the Y_1 output is high.**
- ✓**If ABCD changes to 0100, only the Y_4 AND gate has all inputs high; as a result, only the Y_4 output goes high.**
- ✓**i.e., the subscript of the high output always equal the decimal equivalent of ABCD. Therefore, the circuit is known as binary to decimal decoder**
- ✓**Since it has 4 input lines and 16 output lines, the circuit is also known as a 4 line to 16 line decoder.**



✓IC 74154 is called a decoder-demultiplexer because it can be used either as a decoder or as a demultiplexer.

✓ To use this same IC as a decoder, ground the DATA and STROBE inputs. Then the selected output line is in the low state. i.e., the output line is low when it is active or selected.(Truth table)

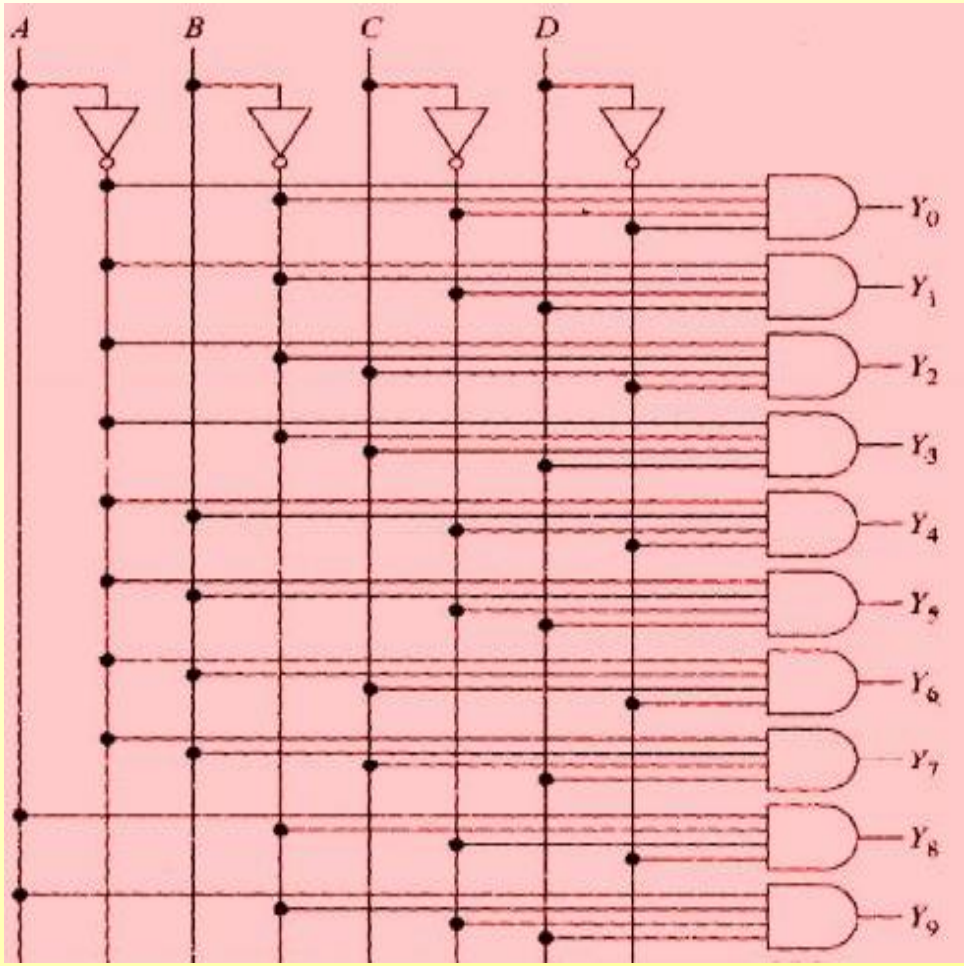
✓For instance, if the binary input is ABCD=0111, then the Y_7 output is low, while all other outputs are high.

Strobe	Data	A	B	C	D	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Truth table of IC 74154

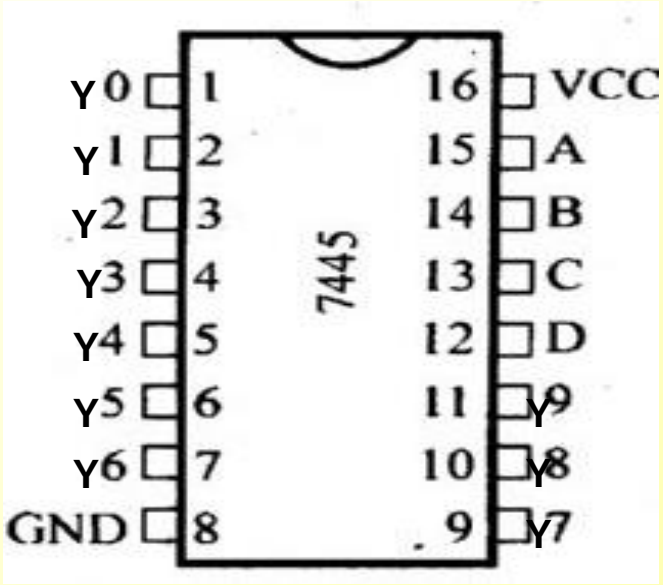
BCD-to-Decimal decoder

The circuit is called a 1-of-10 decoder because only 1 of the 10 output lines is high.



- ✓**For instance , when the input is the BCD code 0011, only Y_3 AND gate has all high inputs, therefore only the Y_3 output is high.**
- ✓**If ABCD changes to 1000, only the Y_8 AND gate has all inputs high; as a result, only the Y_8 output goes high.**
- ✓**i.e., the subscript of the high output always equal the decimal equivalent of the input BCD digit. Therefore, the circuit is also known as BCD to decimal decoder**

IC 7445-BCD to Decimal Decoder



Here pin 16 connects to the supply voltage Vcc and pin 8 is grounded. Pins 12 to 15 are for the BCD input, while pins 1 to 7 and 9 to 11 are for the outputs i.e., Y_0 to Y_9.

✓**This IC is functionally equivalent to the 1 of 10 decoder, except that the active output line is in the low state. All other output lines are in the high state , as shown in the truth table.**

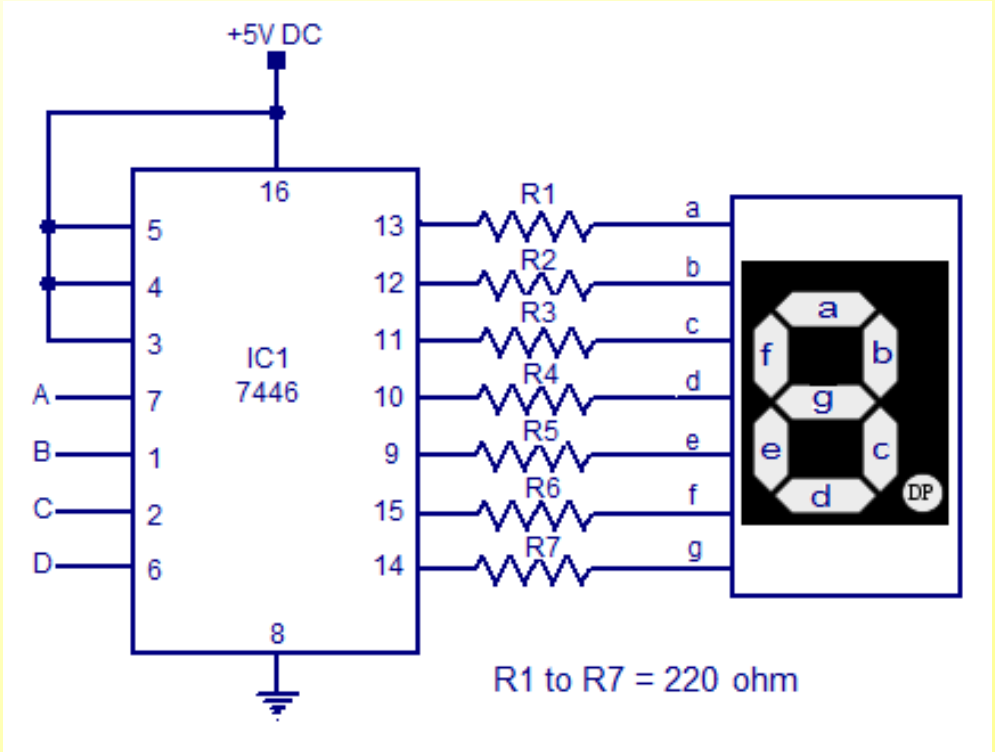
✓**Note that the invalid BCD input (1010 to 1111) forces all the output lines into the high state.**

No.	Inputs				Outputs									
	A	B	C	D	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
Invalid	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

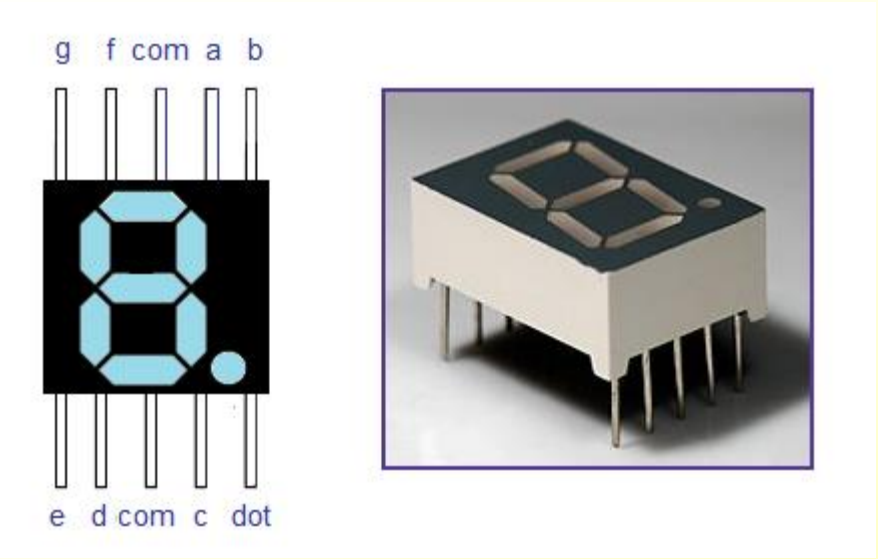
Seven segment Decoder-IC7446

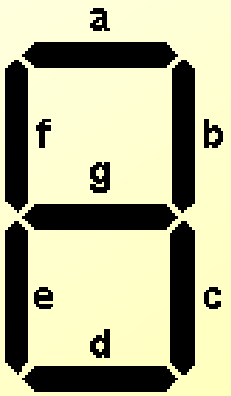
✓A seven segment decoder-driver is an IC decoder that can be used to drive a seven-segment indicator. Here a current limiting resistance is connected between each LED and IC. There are 4 BCD input (ABCD) pins, and 7 output pins (abcdefg).

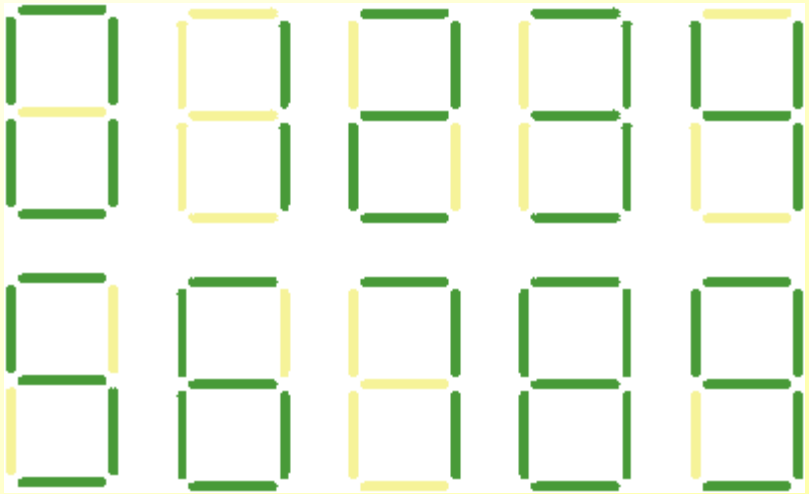
✓The logic circuit inside the IC convert the BCD input to the output. For example, when BCD is 0111, the internal logic logic of 7446 will force LEDs a, b and c to conduct. Hence digit 7 will appear on the seven segment indicator.



Seven segment Display

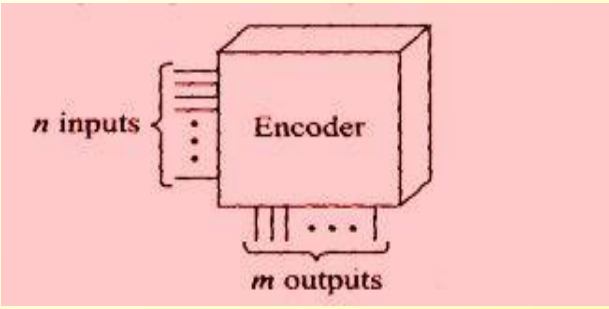






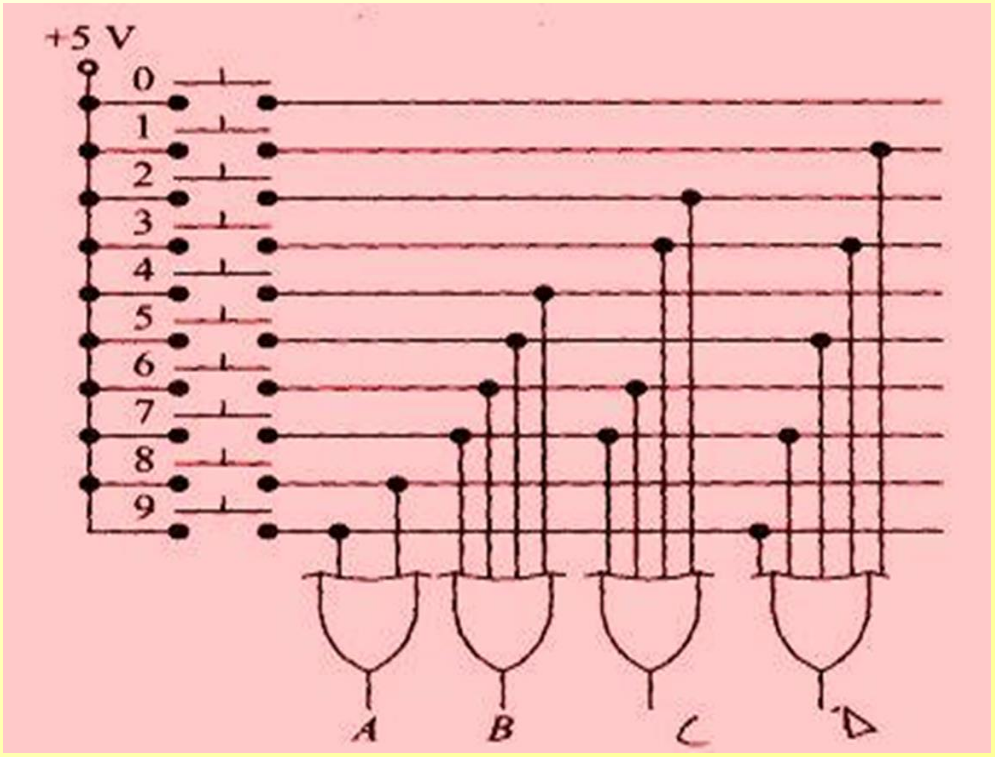
Encoder

An encoder converts an active input signal into coded output signal. There are n input lines, only one of which is active. Internal logic within the encoder converts this active input to a coded binary output with m bits.



Decimal to BCD encoder

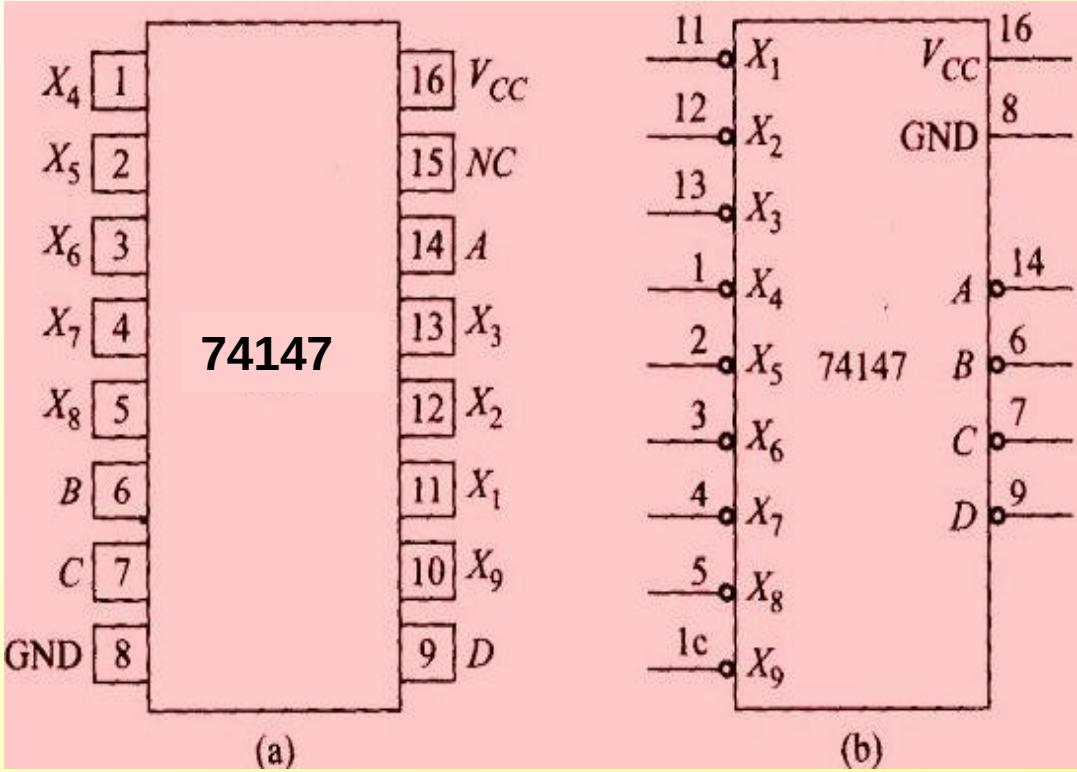
- When button 3 is pressed, the C and D OR gates have high inputs; therefore the output is ABCD=0011.
- If button 5 is pressed, the output becomes, ABCD=0011. Similarly, when switch 9 is pressed, ABCD=1001



IC 74147-Decimal to BCD encoder

✓Figure (a) shows the pin out diagram. The decimal input, X1 to X9, connect pins 1 to 5, and 10 to 13. The BCD output comes from pins 14, 6, 7 and 9. Pin 16 is for the supply voltage, and pin 8 is grounded. NC on pin 15 means no connection.

✓Figure(b) shows the schematic diagram. When all X inputs are high, all outputs are high. When X_9 is low, the ABCD output is LHHL (equivalent of 9). When X_7 is the only low input, ABCD becomes HLLL (equivalent of 7). i.e., an active-low decimal input is being converted to a complemented BCD output.



Truth table of IC 74147-Decimal to BCD encoder

✓**IC74147 is called a priority decoder, because it gives priority to the highest-order input.**

✓**If all inputs X_1 through X_9 are low, the highest of these, X_9 is encoded to get an output of LHHL. In other words, X_9 has priority over all others. When X_9 is high, X_8 is next in line of priority and gets encoded if it is low.**

✓**From the truth table, we can see that the highest active-low from X_9 to X_0 has priority and will control the encoding.**

Inputs									Outputs			
X_1	X_2	X_3	X_4	X_5	X_6	X_7	X_8	X_9	A	B	C	D
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L